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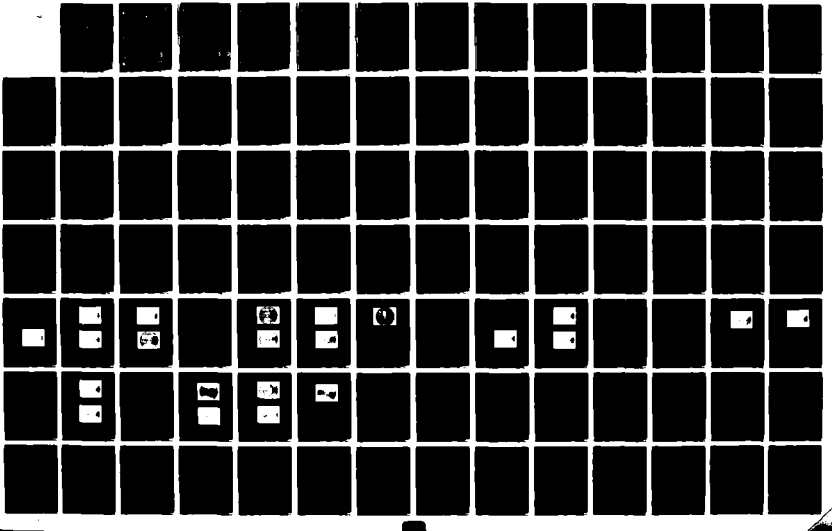

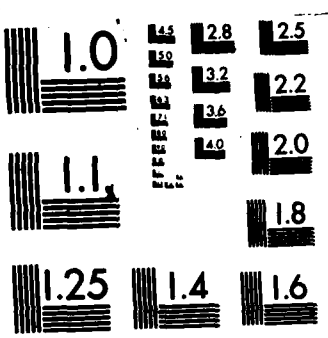

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A MICROSTRIP TIME DELAY CIRCUIT ON BARIUM TETRATITANATE

THESIS

AFIT/GE/EE/83D-25 Danny A. Hahn
Captain USAF

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A MICROSTRIP DELAY CIRCUIT ON BARIUM TETRATITANATE

THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air University
in Partial Fulfillment of the
Requirements for the Degree of
Master of Science

by

Danny A. Hahn, B.S.E.E.
Captain USAF
Graduate Electrical Engineering

December 1983

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Preface

This thesis project explains microstrip techniques as a form of transmission lines. Design equations are presented as well as the complete design for a 1/2 to 8 nsec time delay circuit. The discrete components were selected and tested, and a PIN diode bias control circuit was fabricated. However, although several attempts were made and are described here, transmission lines were never successfully applied to the barium tetratitanate substrate.

Throughout my thesis work, several people provided me with their invaluable assistance, encouragement, and knowledge. Captain Roger Colvin, my advisor, professor, and stimulator was always willing to help me understand the complexities of S-Band circuitry and I am grateful. Additionally, I would like to thank Larry Calahan for his electroplating craftsmanship and Larry Horn for his thick film expertise. Carl Shorte and his men of the AFIT machine shop also gave freely of their specialized talents. A special thanks to my wife Kuniko and our children, Jennifer, Brian, and Mark for their patience, sacrificing and understanding.

Danny A. Hahn

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Major Definitions

The following definitions, although common to many engineers, are provided here because they are basic to an understanding of the problem presented in this thesis.

Dielectric

A dielectric is an insulating material whose dielectric constant may be a function of temperature and frequency. The higher the dielectric constant, the slower an electric wave will propagate through the material; that is, as dielectric constants increase, electric wave propagation velocity decreases.

Permittivity

For a given distribution of charges, the forces between them depend on the environment in which they are located. The greatest force occurs when charges are in free space (vacuum), but the presence of matter reduces this Coulomb force. The permittivity of any dielectric can be expressed as the product of two terms. Thus, if ϵ is the permittivity of any substance and ϵ_0 is the permittivity of free space, then $\epsilon = \epsilon_0\epsilon_r$, where ϵ_r is the relative permittivity of a material substance referred to that of free space. In general ϵ_r *is a complex number.* Its imaginary term can usually be neglected except at very high frequencies. The real term is called the dielectric constant (Ref 5:1-10).

Major Definitions

(Continued)

VSWR

A voltage standing wave ratio (VSWR) is the ratio of maximum to minimum voltage along a transmission line and is a measure of the amount of energy reflected or the amount of mismatch between the line and the load. When the line is perfectly matched and all of the energy is absorbed by the load, the maximum and minimum values are the same, and there is no reflection, i.e. the VSWR is 1.0.

Abstract

A microstrip time delay circuit, variable from 1/2 to 8 nsec in 1/2 nsec increments at a 3 GHz operation frequency with a 10% bandwidth is presented. The temperature stable, miniature circuit is designed for a 50 X 50 X 2 mm substrate of barium tetratitanate, $BaTi_4O_9$.

A PIN diode switching control circuit was fabricated for user selection of the delay time provided by the four-bit loaded switched-line circuit. PIN diodes, chip capacitors, and wound inductors were characterized for this S-Band frequency range.

Several different methods and attempts to adhere a conductor to the barium tetratitanate substrate were made and are presented here, however the complete time delay circuit was never fabricated.

A MICROSTRIP TIME DELAY CIRCUIT ON BARIUM TETRATITANATE

I. Introduction

Background

Phased array radars need low cost, temperature stable, variable time delay units at frequencies including three gigahertz. Variable time delay units provide the means to change the relative time of the signals transmitted from each element of an antenna array. These relative time variations allow the radar beam to be steered in a desirable direction (Ref 12:24). Typical military radar systems require a variable time delay of up to 100 nanoseconds. For example, Figure I-1 depicts a phased array radar antenna 120 feet wide with the desired direction of propagation at an angle of 30 degrees from the face of the antenna. For each radiating element to be in phase at a line normal to the propagation vector requires a successively smaller time delay from each element. In this example, the wave from the left-most element must travel (120 feet)(cos 30) = 104 feet farther than a wave from the right-most element. Additionally, after traveling this 104 extra feet, it must be in phase with the wave just leaving the right-most element. In free space, this electromagnetic wave takes approximately one nanosecond per foot of travel. Thus the

104 foot difference corresponds to approximately 104 nanoseconds of delay across the face of the antenna.

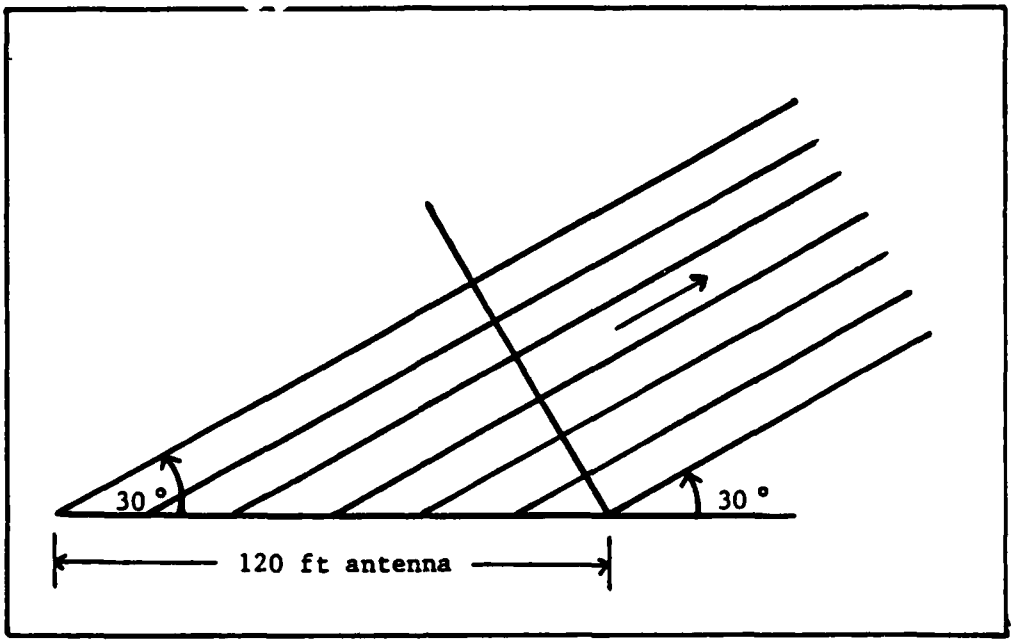

Figure I-1, Phased Array Antenna

One approach to this problem uses sections of coaxial cable of various lengths, and is called a tapped electromagnetic delay line. Different time delays are obtained by electronically selecting and routing the signal through the proper length of cable (Ref 18:401). An 8 nanosecond time delay requires a section of coaxial cable approximately 5.5 feet long (Ref 8:67-74). For an array antenna consisting of thousands of elements, each of which may require a different time delay, this method is very bulky and undesirable.

Microstrip design techniques provide a method of

miniaturization. The microstrip consists of a flat metallic strip conductor bonded to a dielectric sheet which is in turn bonded to a metallic ground plane. The tapped delay line principle is the same; that is, different electrical transmission paths are electronically selected from a group of transmission lines printed on a substrate (the dielectric sheet). The different lengths of transmission lines yield different time delays. Unfortunately, these microstrip time delay units are usually temperature sensitive. Nonetheless, economical circuits using microstrip have been implemented in many low to medium power radars and their associated electronic countermeasures, some segments of point-to-point radio links, and certain portions of satellite communications systems (Ref 4:17).

Summary of Current Knowledge

Variable time delay circuits have been fabricated on substrates other than barium tetratitanate (Ref 3:268-269), and fixed time delay circuits have been fabricated on barium tetratitanate (Ref 9:419). However, a review of the literature has shown that no one has fabricated a variable time delay on barium tetratitanate.

Barium tetratitanate made its debut in 1971 and has been fairly well documented as a low loss, temperature compensated dielectric with a high dielectric constant suitable for microwave applications (Ref 13:1628). A variable time delay circuit on barium tetratitanate was

researched and designed last year for an AFIT thesis (AFIT/GE/EE/82D-21), however, only test circuits on alumina substrates were fabricated.

Microstrip technology has been in use for at least 15 years and numerous articles are available in the technical literature. Over 130 references on microstrip analysis and design are listed in the book by Gupta, Garg, and Bahl (Ref 7).

Problem

Using microstrip techniques, this project will be an attempt to construct a variable time delay circuit of meandering transmission lines on a two inch square substrate of barium tetratitanate, a material with a high dielectric constant which is relatively unaffected by temperature variations. The purpose of this project will be to prove the accuracy of dependable, miniature, temperature compensated time delay circuits for signals propagating at 3 GHz.

Scope

The scope of this project will be limited in the following manner. This time delay unit will be variable from one-half to eight nanoseconds in one-half nanosecond increments. It will be fabricated using only single layer designs, therefore, only discrete chip components (resistors, diodes and capacitors) will be used as connecting elements, and printed components will not be

used. The primary consideration will be to obtain a constant voltage standing wave ratio (VSWR) as temperature varies and to minimize this VSWR. Since the VSWR is greatly affected by discontinuities in the transmission line, such as those caused by attaching the connecting elements, particular care will be given to this aspect of the problem.

The project was sponsored by Dr. Paul H. Carr, Electromagnetic Science Division, Antennas and RF Components Branch, Rome Air Development Center, Hanscom Air Force Base, Ma.

Assumptions

The assumptions made regarding this thesis are listed below.

1. Standard published design equations and microstrip fabrication techniques were assumed accurate enough for this project.
2. The manufacturer's material specifications (dielectric constants, temperature coefficients, junction thermal resistance, etc.) provided were assumed accurate.
3. Subcircuits of this project were designed last year as thesis project AFIT/GE/EE/82D-21 (Ref 1). These research results were assumed to be valid. Preliminary verification was accomplished, and a minor redesign of some subcircuits was required.
4. All equipment listed in appendix A was assumed to

be properly calibrated.

Approach and Standards

The chronological approach taken in this project is listed below.

1. Electroplate a ground plane on the back surface of the alumina microstrip substrates fabricated for testing purposes last year. This was necessary to achieve a constant VSWR. Last year's circuits had a varying VSWR.
2. Verify a good (low VSWR) 50 ohm transmission line with a 3 GHz input signal. A good transmission line is fundamental to any time delay circuit.
3. Add capacitors to the transmission line. Different values of capacitance and different mounting techniques were explored until the VSWR was minimized.
4. Add series diodes to the circuit. Various mounting techniques were tried until a minimum VSWR was achieved under forward bias, and high isolation was obtained under reverse bias.
5. Attach radio frequency coils in shunt to the transmission line to pass the DC diode biasing current and reflect the incident RF power. Different values of inductance were attempted until a value was found such that the coil appeared as an open circuit to the RF and had a minimal effect on

the transmission line.

6. Verify the transmission line spacing on the existing test circuits for electromagnetic coupling effects. There should be minimum coupling between the meandering legs of the transmission line.
7. Construct the diode switching control circuitry to allow a user to select the desired time delay.
8. Fabricate the transmission line patterns on a barium tetratitanate substrate.
9. Attach the previously determined, optimally valued components.
10. Switch between various lengths of meandering transmission line to demonstrate variable time delays with minimized VSWR.

Summary

This chapter provided background material on the need for low cost, temperature stable, variable time delay circuits in the S-Band frequency region. Barium tetratitanate, a temperature compensated, ceramic dielectric, was presented as the substrate to be used with microstrip technology. The specific problem addressed was to construct switchable meandering transmission lines on a two inch square of this substrate.

In the following chapter, specifications of the time delay circuit, microstrip qualities and barium tetratitanate characteristics are discussed. This is followed by

transmission line design equations, PIN diode characteristics, and the overall time delay circuit design. The third chapter describes circuit and component fabrication, testing, and results, followed by a chapter on the processing of barium tetratitanate substrates to apply a microstrip circuit. The final chapter includes conclusions and recommendations for future work.

II. Circuit Design and Theory

This chapter details the variable time delay circuit specifications and the microstrip method of transmitting a microwave signal. The characteristics of barium tetratitanate, the substrate material, are explained, and design equations are presented to supply the parameters necessary to fabricate a transmission line on this substrate. PIN diodes, the switching elements used to select different time delays, are discussed, followed by the entire time delay circuit design. Finally, RF isolation and power handling limits of the final design are theoretically derived and calculated.

Specifications

The circuit specifications, provided in part by the project sponsor, are listed below.

1. User Variable Time Delay. Using digital control, the circuit will allow the user to select a time delay ranging from one-half to eight nanoseconds in one half nanosecond increments.
2. S-Band Operating Frequency. The application for this time delay unit is in phased array radar systems, therefore the operating frequency of the circuit will be 3 GHz.
3. Broad Band Transmission Line. In this circuit, broad band is defined to be ten percent. This circuit will

have a bandwidth of 300 MHz and have good characteristics from 2.85 GHz to 3.15 GHz.

4. Temperature Stable. Temperature variations will have a negligible effect on frequency and time delay.
5. Miniature. This time delay circuit will be integrated on a two inch by two inch by 0.08 inch barium tetratitanate substrate provided by the sponsor.

Microstrip Qualities

The microstrip line as it is used today in microwave integrated circuits represents the second generation of printed transmission lines. The original version, called stripline, was introduced in 1949. In 1955, microstrip evolved and much interest was expressed in this new form of transmission line for a few years after its introduction. However, its use in microwave design did not become very popular until the mid-1970s when new low-loss dielectric and ferrite substrate materials became available (Ref 14:67-68).

Microstrip is an extremely useful transmission line medium for use at frequencies from a few gigahertz through tens of gigahertz. The geometry of a microstrip transmission line is shown in Figure II-1.

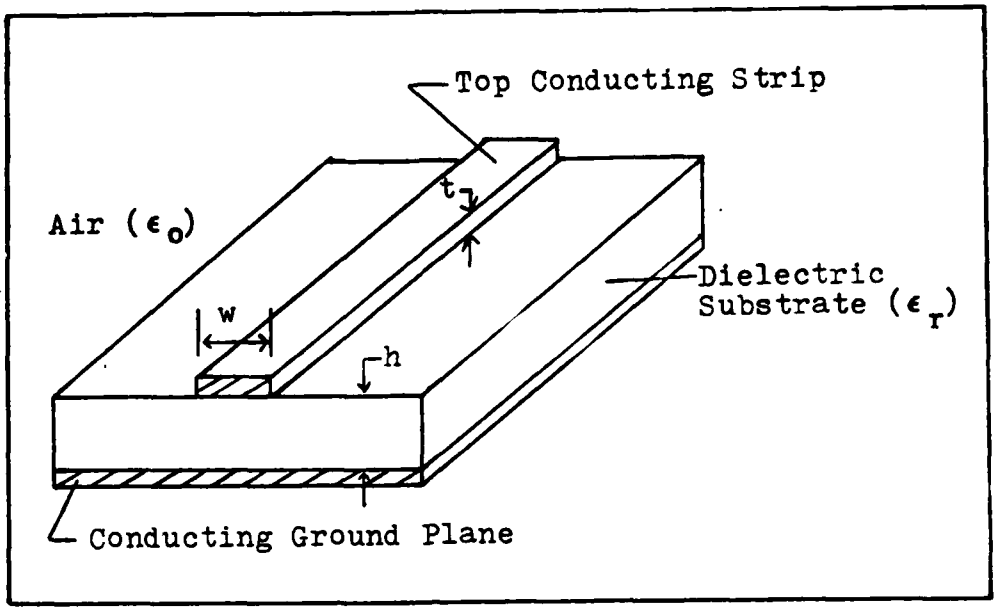

Figure II-1, Microstrip Line

The most important parameters are the microstrip width (w) and the thickness of the substrate (h). Also important is the relative permittivity of the substrate (ϵ_r). The thickness of the metallic, top conducting strip (t) is generally of much lesser importance.

Some of the particularly useful characteristics of microstrip include the fact that active and passive devices such as diodes, transistors, and capacitors, can be readily incorporated into the circuit. Additionally, direct current as well as radio frequency signals may be transmitted. This is extremely convienent for the biasing of PIN diode switches. In-circuit characterization of devices is easy to implement. The line wavelength is reduced considerably from its free-space value, because of the substrate dielectric

concentrating the fields. This allows distributed component dimensions to be relatively small. Finally, the structure is quite rugged and can withstand moderately high voltage and power levels (Ref 4:34-36).

Barium Tetratitanate

Barium tetratitanate ($BaTi_4O_9$) is a ceramic that was developed for its special dielectric properties. It is temperature stable with a dielectric temperature coefficient of -3.67 ppm/^{o}C from -20 to +60 ^{o}C. It has a high relative dielectric constant of 36.97 (Ref 2). The material can be formed by hot pressing or by a fired process, has excellent reproducibility, and currently is manufactured by Thomson-CSF of France, Trans. Tech of Maryland, and Murata of Japan. Different manufacturers list relative dielectric constants from 36.26 to 38.26, with an average dissipation factor or loss tangent ($\tan \delta$) of 0.00039. The fractional temperature coefficients range from -52.9 to -3.67 ppm/^{o}C, and the thermal conductivity is 2.0934 watts/m ^{o}C.

By comparision, alumina, another popular dielectric has a relative dielectric constant of 9.8, a loss tangent of 0.0005, a temperature coefficient of +136 ppm/^{o}C, and a thermal conductivity of 29.308 watts/m ^{o}C (Ref 13:1628; 10:659-660).

For time delay circuit applications, the use of barium tetratitanate compared to alumina has two obvious advantages. The high relative dielectric constant allows

the printed transmission lines to be both shorter in length and smaller in width on the barium tetratitanate than on the alumina for a given time delay. This helps meet the design specification of being miniature. Additionally, the lower dielectric temperature coefficient provides a very stable relative dielectric constant over a wide temperature range. This factor is the key in the design specification for temperature stability.

Transmission Line Design

The design of a microstrip transmission line involves the width of the top conductor (w), the thickness of the substrate material (h), and the relative dielectric constant (ϵ_r). The line width to substrate thickness ratio determines the characteristic impedance (Z_0) of the transmission line. The physical length of the transmission line is proportional to the electrical length or the wavelength of a signal propagating through the substrate. Therefore, the physical length of the microstrip line will determine the time delay.

The substrates provided for this project are nominally two millimeters thick and have a relative dielectric constant of 36.97. For compatibility with the time delay circuit's proposed environment (and the availability of existing test equipment) the design characteristic impedance will be fixed at 50 ohms. These known values are applied to various design equations to find the w/h ratio, from which

the width (w) of the transmission line can be determined. There are several different approaches and versions of these design equations.

Bellacicco, in his thesis (Ref 1) used a version of the design algorithm presented by Gupta which is shown below. Gupta states these expressions provide an accuracy better than two percent (Ref 6:61-62).

For $A > 1.52$

$$w/h = 8 \exp(A) / (\exp(2A) - 2) \quad (1)$$

while for $A < 1.52$

$$w/h = (2/\pi)\{B - 1 - \ln(2B - 1) + ((\epsilon_r - 1) / (2\epsilon_r))(\ln(B - 1) + 0.39 - (0.61 / \epsilon_r))\} \quad (2)$$

where

$$A = (Z_0 / 60)((\epsilon_r + 1) / 2)^{1/2} + ((\epsilon_r - 1) / (\epsilon_r + 1))(0.23 + 0.11/\epsilon_r) \quad (3)$$

and

$$B = (60 \pi^2)/(Z_0 (\epsilon_r)^{1/2}) \quad (4)$$

With Z_0 fixed at 50 ohms and $\epsilon_r = 36.97$, equation (3) gives a value of $A = 3.852$. This implies equation (1) should be used. Substituting A into equation (1) gives a value of $w/h = 0.17010$. Since the substrate is two millimeters thick ($h = 2.0$ mm), w, the width of the transmission line, is 0.340 mm for a 50 ohm line on this substrate. These results

assume the microstrip line thickness (t) to be negligible. Actually the strip thickness affects the characteristics, but when $t/h < 0.005$, Gupta reports the agreement between experimental and theoretical results, obtained by assuming $t/h = 0$, is excellent. These equations also assume the microstrip circuit has no cover.

Sensitivity Analysis

Suppose the substrate is not flat, but instead varies in height, h, from 1.9 mm to 2.0 mm, a five percent variation. If the design width, w, of the transmission line is 0.340 mm then $w/h = 0.340/1.9$. Using this value and solving equation (1) for A, and then equation (3) for Z_0 provides a value of $Z_0 = 49.3$ ohms. Thus, a five percent change in the substrate's height produces a 1.4 percent change in the transmission line's characteristic impedance.

Relative Effective Dielectric

The microstrip line (see Figure II-1) is an inhomogeneous transmission line because the field lines between the strip and the ground plane are not contained entirely within the substrate. The microstrip line sees a relative dielectric of air ($\epsilon_r = 1$) above and a relative dielectric of the substrate ($\epsilon_r = 36.97$) below. The presence of this substrate - air dielectric interface modifies the mode of propagation in microstrip. To account for this dielectric discontinuity, a quantity called the relative effective dielectric constant (ϵ_{re}) is used in

microstrip design equations. This quantity is unique to mixed - dielectric transmission line systems and provides a useful relation between various wavelengths, impedances, and propagating velocities.

The relative effective dielectric constant is always lower than the dielectric constant of the substrate. Gupta reports the following formula for ϵ_{re} has a maximum relative error of less than two percent (Ref 6:61).

$$\epsilon_{re} = (\epsilon_r + 1)/2 + ((\epsilon_r - 1)/2)(1 + 10h/w)^{-1/2} \qquad (5)$$

From above, with h/w = 5.8787 and ϵ_r = 36.97, the value from equation (5) is ϵ_{re} = 21.31.

The propagating wavelength in a microstrip circuit, λ_m, is related to ϵ_{re} as follows:

$$\lambda_m = \lambda_0/(\epsilon_{re})^{1/2} \qquad (6)$$

where λ_0 is the free space wavelength. For the 3 GHz specification frequency, λ_0 = 100 mm, which when substituted into equation (6) gives λ_m = 21.66 mm.

For any propagating wave the velocity is given by the appropriate frequency - wavelength product. In free space we have $c = f\lambda_0$, and in microstrip the velocity of propagation $v_p = f\lambda_m$.

At 3 GHz, $v_p = 6.499 \times 10^7$ meters/sec, therefore, a time delay circuit on a barium tetratitanate substrate,

will require 64.99 mm (2.6 inches) of microstrip for a one nanosecond delay. By comparison, coaxial cable would be 210 mm (8.3 inches) long for this same time delay.

Skin Depth

At high frequencies, electric current is mainly conducted near the surface of the conductor. The depth at which the current density falls to 1/e of its value at the surface is called the skin depth, δ. This skin depth is given by White (Ref 18:65-66) as:

$$\delta = (\pi f \mu_0 \sigma)^{-1/2} \qquad (7)$$

where

f = operating frequency

$\mu_0 = 4 \times 10^{-7}$ Henry/m = free space permeability

σ = conductivity (ohm - meters)$^{-1}$

With the conductivity of gold = 4.10×10^{7} /(ohm - meters), the skin depth is then 1.44 microns.

Edwards (Ref 4:28) recommends a minimum of four skin depths for the thickness (t) of the microstrip conductor. Other authors (Ref 14:17) require three to five skin depths, while Gupta, as previously mentioned, requires t/h <0.005 for his design equations. Thus the thickness (t) of the conductor should be between 4.32 and 10 microns. For easy reference, a summary of these design parameters and values is shown in Table II-1.

Table II-1, Summary of Microstrip Design Parameters

Parameter	Value
Substrate Material	Barium Tetratitanate
Thermal Conductivity (K)	2.0934 watts/(m ^{o}C)
Surface Dimensions	50 X 50 mm
Thickness of Substrate (h)	2.0 mm
Dielectric Constant (ϵ_r)	36.97
Characteristic Impedance (Z_0)	50 ohms
w/h Ratio	0.17010
Width of Microstrip (w)	0.340 mm
Relative Effective Dielectric Constant (ϵ_{re})	21.31
Wavelength at 3 GHz (λ_m)	21.66 mm
Length of Microstrip for 1 nsec. delay	64.99 mm
Thickness of Conductor (t)	4.32 to 10 microns
Spacing to Width Ratio	3 : 1

PIN Diodes

A PIN diode is a semiconductor device with a heavily doped p region and a heavily doped n region separated by a layer of high resistivity material that is nearly intrinsic, hence the acronym PIN. Electrical contact is made to the two heavily doped, low resistivity, regions. The PIN diode was first proposed over 30 years ago (1952) as a low frequency rectifier that could rectify more power than a simple p-n junction diode. Although it is a poor rectifier at frequencies above a few megahertz, the PIN diode can be used for other purposes in many microwave applications.

With zero or reverse bias, the PIN diode has a very high impedance to microwave frequencies, while at moderate forward bias current it has a very low impedance. These characteristics permit the use of a PIN diode as a switch in a microwave transmission line (Ref 15:271-272). A schematic equivalent of an unpackaged PIN diode chip is shown in Figure II-2 (Ref 18:69). When it is forward biased, the PIN diode will pass microwave signals from either direction. However, even though the PIN diode is nearly nonconducting at zero bias, reverse bias is necessary to fully deplete the I region and its boundaries of charge. Reverse bias under high RF voltage stress has a second role, that is, it must remove small amounts of charge which may be injected into the I region during the forward going excursion of the RF waveform. This charge, though small, could be multiplied by impact ionization of the RF voltage excitation, resulting in

thermal runaway of the diode, increased RF losses and possible destruction. The extraction of such charge is called the "pulse leakage current", since it occurs only under the combined action of RF and reverse bias excitation. To protect the diode, the bias driver must be capable of providing this pulse leakage current without an appreciable drop in voltage supplied (Ref 17:663-664).

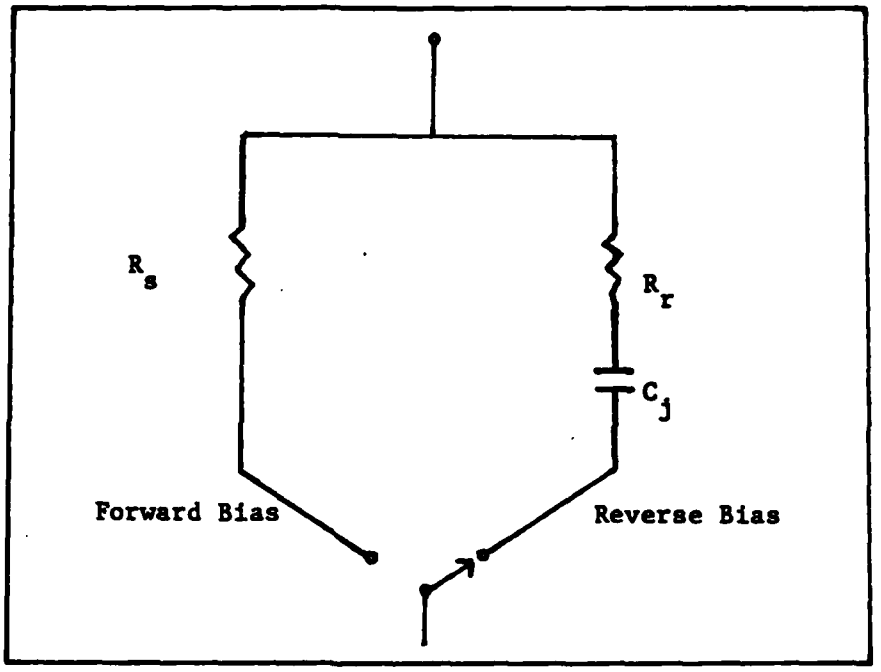

Figure II-2, PIN Diode Chip Equivalent Circuit

Two different PIN diodes, MA-4P202-134 and MA-4P404-134, were available for this thesis project. Both are in chip form and are manufactured by Microwave Associates. The 4P202 diode has a junction capacitance of 0.05 pF compared to 0.20 pF for the 4P404 (Ref 16:107,116). The isolation that must be provided by the reversed biased

diode is a function of this junction capacitance and is defined by White (Ref 18:147) as follows.

$$\text{Isolation} = 10 \log (1 + X_c/(2Z_0))^2 \qquad (8)$$

Using equation (8), at 3 GHz, the 4P202 provides 21.3 dB of isolation, while the 4P404 provides 11.3 dB. Therefore, the 4P202 provides a better "off" condition, and was the diode selected for this project.

The insertion loss presented by a forward biased PIN diode is the ratio of the power available, to the power dissipated in the load. White (Ref 18:147) presents this insertion loss as follows.

$$IL = (1 + R_s/(2Z_0))^2 \qquad (9)$$

R_s, the series resistance of a forward biased PIN diode decreases exponentionally with the forward bias current. From the 4P202 specification sheet (Ref 16:107), for a forward bias current of 10 ma, R_s = 2.0 ohms. Using equation (9), this gives an insertion loss of 1.040 (0.17 db) or 4 percent of the applied power is dissipated in the diode. Increasing the forward bias current to 20 ma makes R_s = 1.5 ohms, which is an insertion loss of 1.030 (0.13 db) or 3 percent dissipation in the diode. For forward bias currents from 50 to 100 ma, R_s remains fairly constant at 1.1 ohms for an insertion loss of 1.022

(0.095 db). Therefore, to keep the current as small as possible, yet provide for reasonable insertion loss, the design forward bias current is 20 ma.

Time Delay Circuit Design

The fundamental configuration for this project consists of various lengths of transmission line and a switching network. The desired time delay is selected by electronic switching of cascaded line sections in such a manner that the total transmission line length corresponds to the desired delay.

Bellacicco has shown the N-bit loaded switched delay line design to be more efficient that either a tapped delay line or an N-bit switching network (Ref 1:59).

The tapped delay line network consists of one long transmission line with several taps along its length. Some of the taps are used for input and some for output. A simple example of a tapped delay line is shown in Figure II-3. The primary disadvantage of this configuration is that the losses for different delay times will vary greatly due to the varying number of diode switches seen by the RF signal.

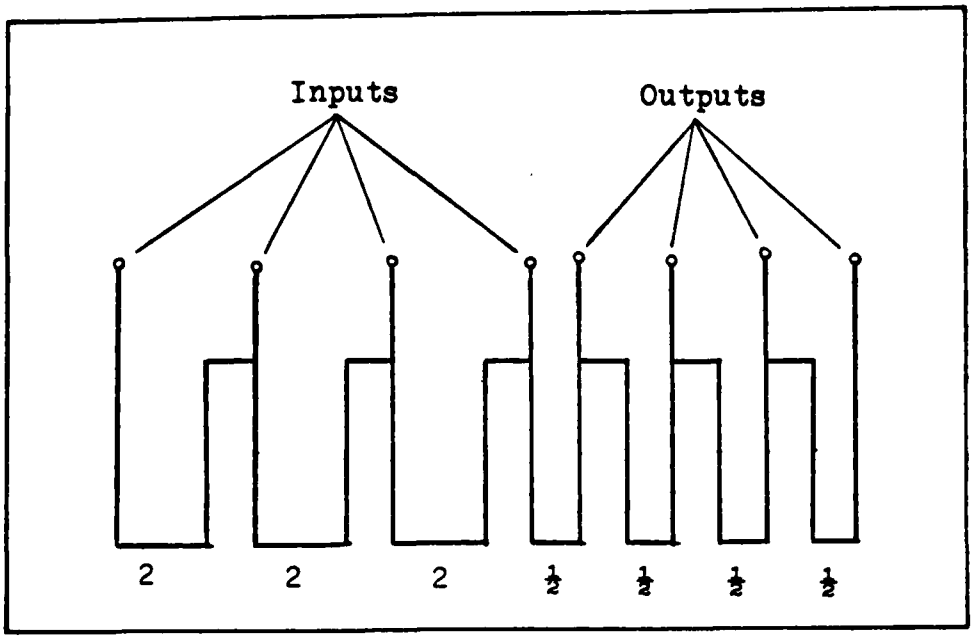

Figure II-3, Simple Tapped Delay Line

The N-bit switched delay line has two electrically parallel transmission lines of different lengths for each bit. Switching diodes are used to select one path or the other. A cascaded combination of N bits can yield up to 2^N different delays. A variable time delay circuit from one-half to eight nanoseconds in one-half nanosecond increments requires 16 different delays. This corresponds to 2^4 or a 4-bit design.

A simple example of a 4-bit tapped delay line is shown in Figure II-4. The primary disadvantage of this design involves resonances and poor isolation in the switched-out path. If the long path in any particular bit is longer than $\lambda_m/2$ for the frequency of operation, it can resonate (Ref 18:392; 11:694). A small amount of RF energy can be

capacitively coupled through the switched-off diode and set up a resonance, with a frequency dependent upon the length of this switched-out line. A fraction of this resonant energy will be coupled out to the rest of the circuit. Isolation could be increased by adding more diodes at each end of the long path but these extra diodes would increase the insertion loss when the long path is switched in.

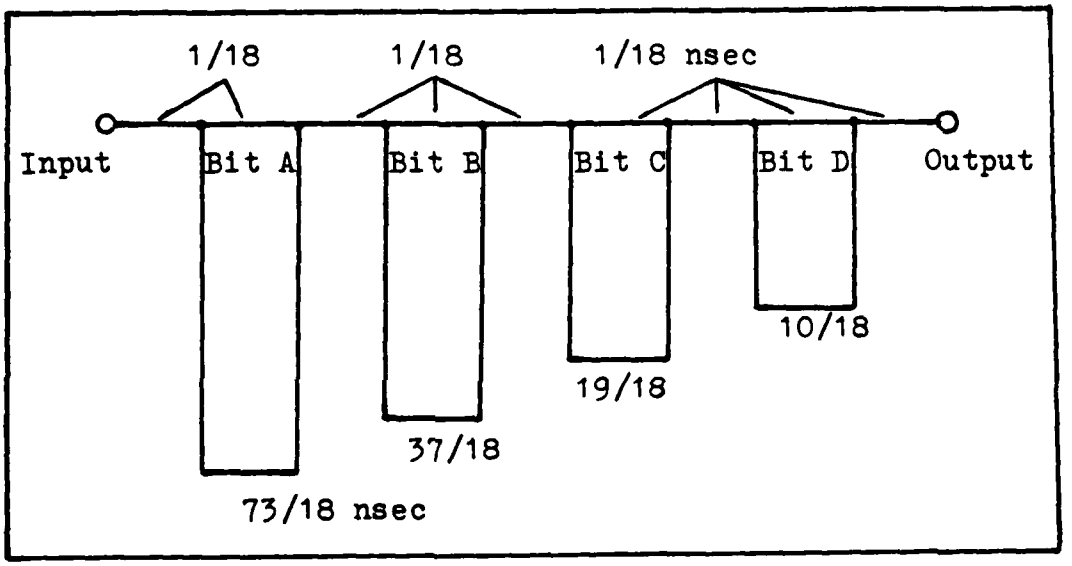

Figure II-4, Simple 4-Bit Switched Delay Line

The N-bit loaded switched delay line is similar to the unloaded example described above except the unused long delay line portions are terminated in their characteristic impedance. A diagram of a one bit loaded delay circuit is shown in Figure II-5. By loading the unused path with its characteristic impedance, any resonance that might occur is effectively dampened. Of course, some power will still be

coupled to the long path when it is the switched-out path, but since the line is no longer resonant, the amount of power coupled over will be minimal (Ref 11:693-694). The schematic of a 4-bit loaded switched-line delay circuit is shown in Figure II-6. This schematic is the basis for this thesis and was the design used in circuit fabrication.

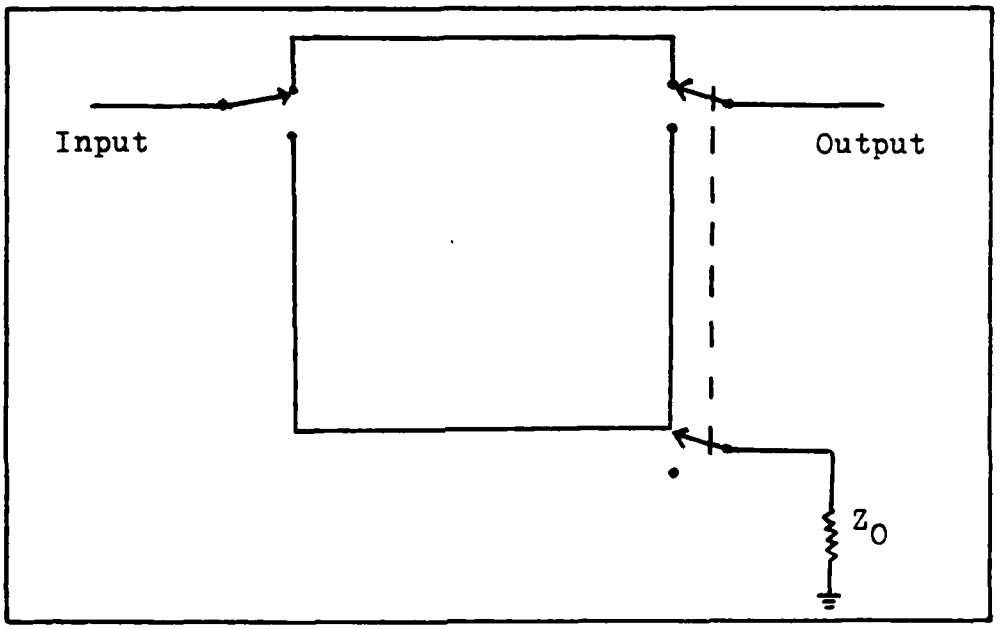

Figure II-5, One-Bit Loaded Switched-Line Delay Circuit

The theory of operation of Figure II-6 is best explained by examining only one bit. All the rest are identical. Consider Bit A to be configured for the minimum delay, i.e. the top path switched in and the bottom path switched out. To obtain this condition, "A" is high (+5 volts) and "$\bar{A}$" is low (-50 volts). This high on "A" forward biases diodes D1 and reverse biases diodes D2. The -V terminal is always held low (-50 volts) to provide about -25

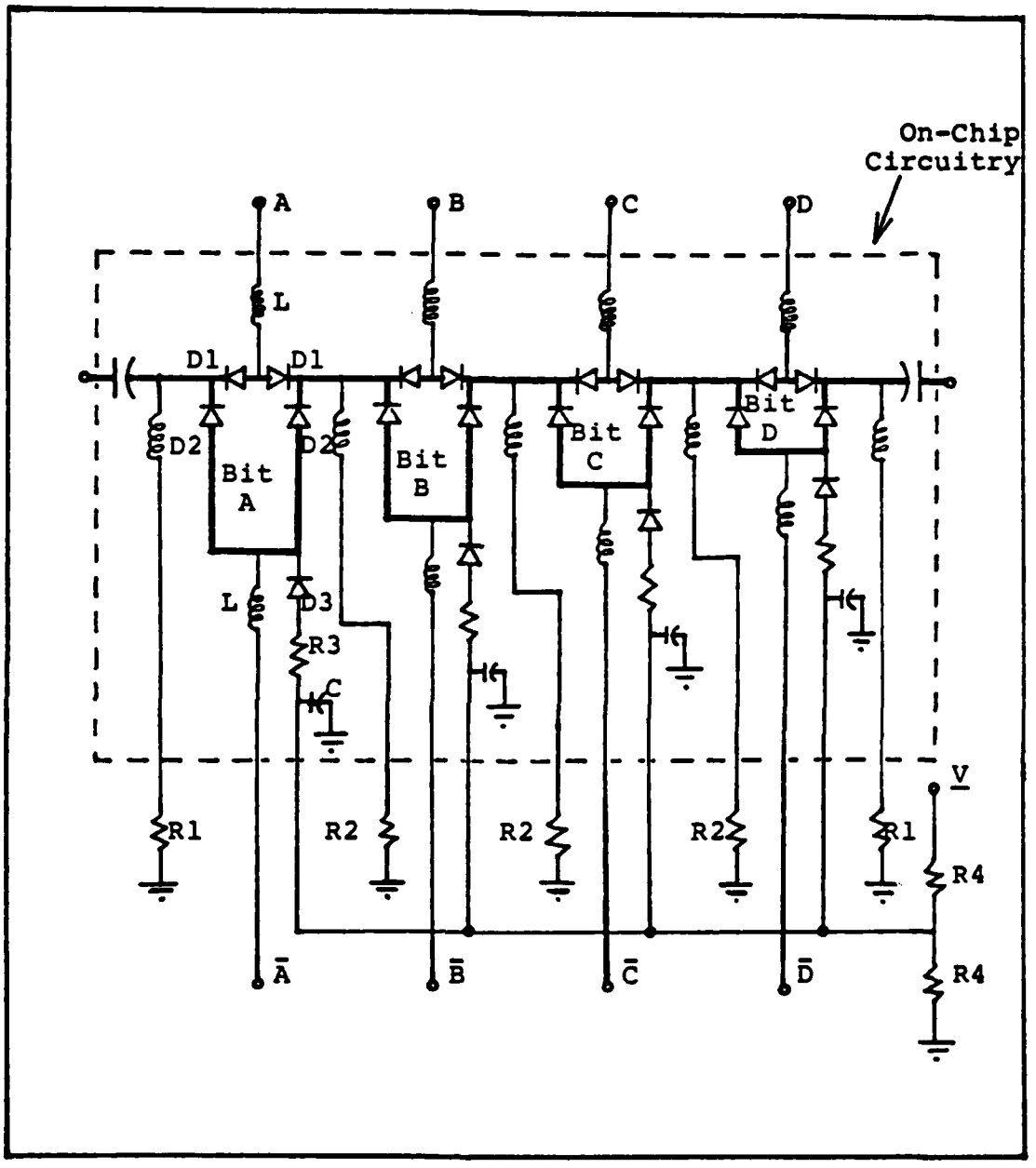

Figure II-6, Four-Bit Loaded Switched-Line Schematic

volts, through the voltage divider resistors R4, to the anode of diode D3. The low on "$\bar{A}$" forward biases diode D3 and helps reverse bias diodes D2. The diodes D2 block the RF signal from the long path of Bit A, and D3 allows this unused long path to be terminated in its characteristic impedance (R3). With diodes D1 forward biased, the RF signal passes along the short path. DC bias current from the diode switching control system flows through control line "A", the RF coil (RFC), diodes D1, and through a RFC and R1 or R2 on either side of the bit to ground.

In the maximum delay configuration for Bit A, "A" is low (-50 volts), which reverse biases diodes D1, effectively switching out the short path. "$\bar{A}$" is high (+5 volts), which forward biases diodes D2 and reverse biases diode D3. The long path is no longer terminated in its characteristic impedance and the RF signal follows this long path through Bit A.

All bias resistor values were chosen to provide a nominal forward bias current of 20 ma. The capacitors are required to route these bias currents to the PIN diodes only, and they present minimum impedance to the RF signal. Conversely, the RF coils present a high impedance to the RF signal and are necessary to keep RF from reaching the DC bias supply. A summary of these component values is shown in Table II-2.

Table II-2, Component Summary

Component	Value	Quantity	Style
R1	220 ohms	2	1/4 watt
R2	110 ohms	3	1/4 watt
R3	50 ohms	4	Chip
R4	2200 ohms	2	1/4 watt
C	100 pF	6	Chip
RFC	30 nH	13	Hand Wound

The actual physical layout for this time delay circuit is shown in Figure II-7. Note that all DC switching and bias control lines are on the bottom edge of the substrate while the RF enters and exits the top edge. A cross sectional view depicting the mounting techinque for the chip components is shown in Figure II-8

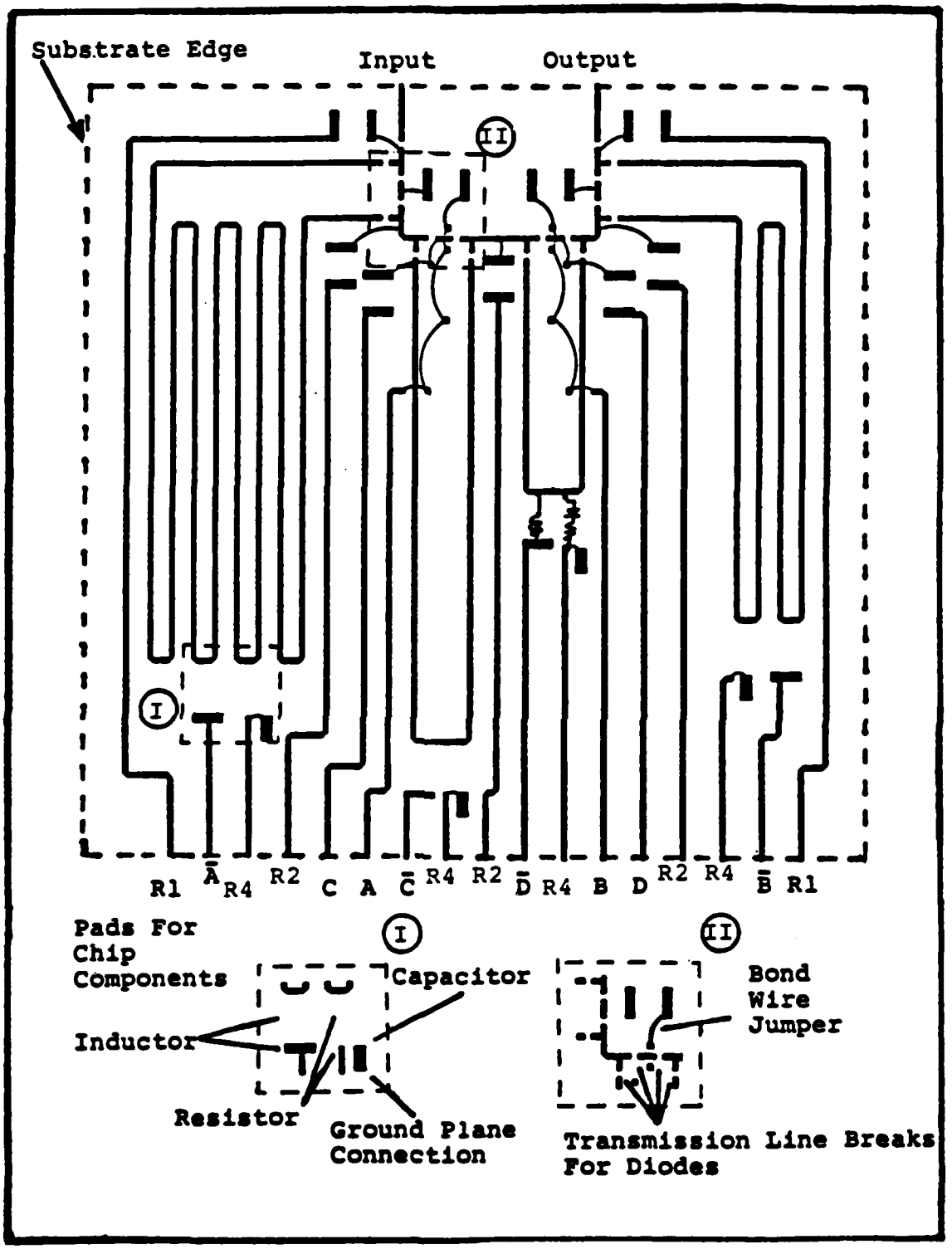

Figure II-7, Physical Layout of Circuit

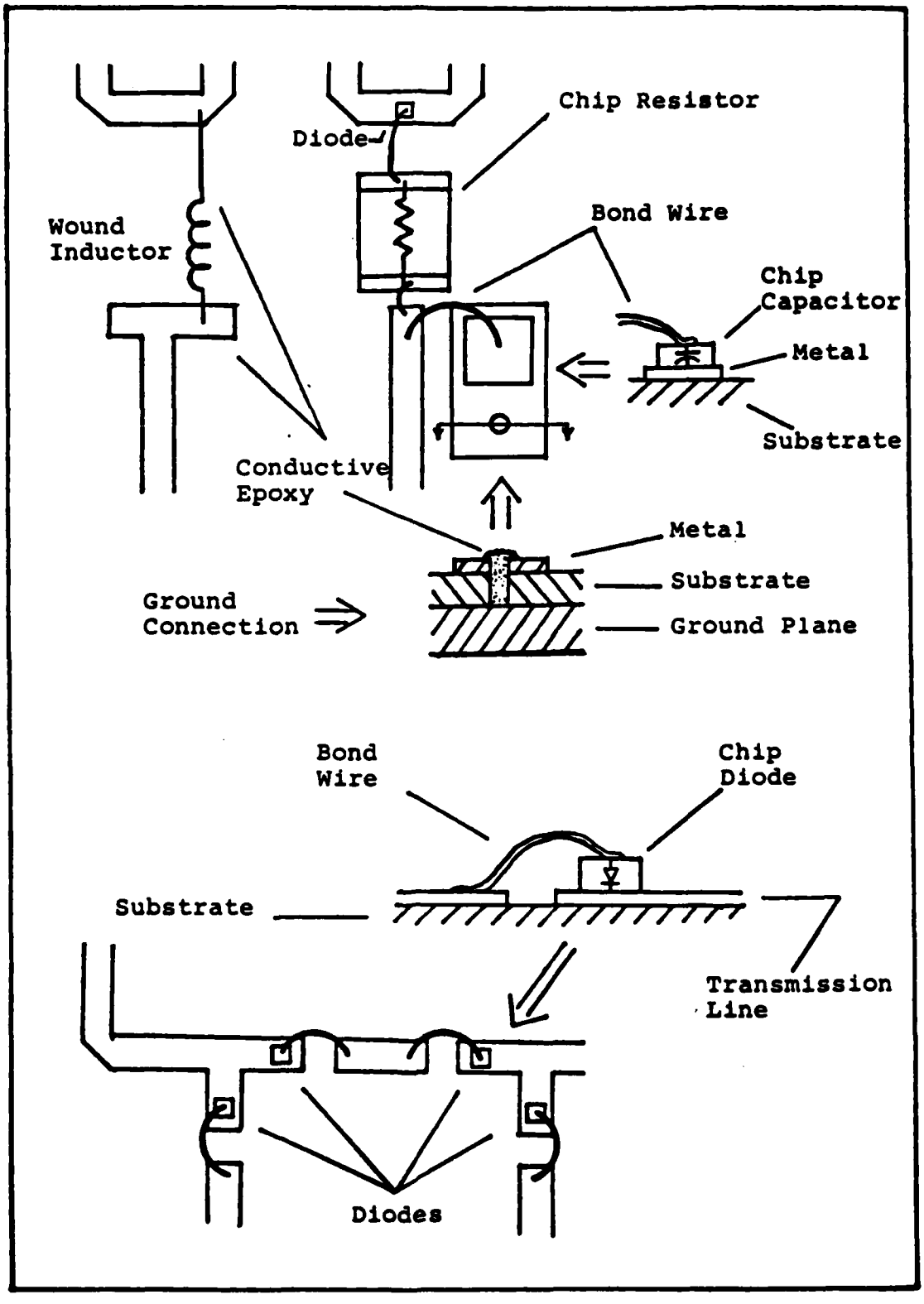

Figure II-8, Component Mounting Detail

Switching Control Circuit

The control circuit for the time delay transmission line consists mainly of four double-pole double-throw switches and the biasing resistors. There is one switch for each bit of the time delay circuit, each wired in such a manner that when "A" is high (+5 volts), "$\bar{A}$" must be low (-50 volts), and vice-versa. All control lines are connected to 17 of the bottom 25 pins of a 50 pin wire wrap header. Complete details of this switching control circuit are given in the next chapter.

Isolation

To determine the required isolation that must be provided by the reverse biased diodes in the switched-out paths, the maximum allowable error for the entire circuit must be specified. This time delay circuit ranges from 1/2 through 8 nsec in 1/2 nsec increments. Allowing 2% of this increment or 10 picoseconds as the total error in the time delay circuit, the maximum phase angle error is 10.8^0 as shown below.

Recalling that in this microstrip, $v_p = 6.499 \times 10^7$ m/sec and $\lambda_m = 21.66$ mm we have:

$$(6.499 \times 10^7)(10 \text{ picosec})(360^\circ/21.66 \text{ mm}) = 10.8^\circ \quad (10)$$

Now, referring to Figure II-9, assume zero error is the

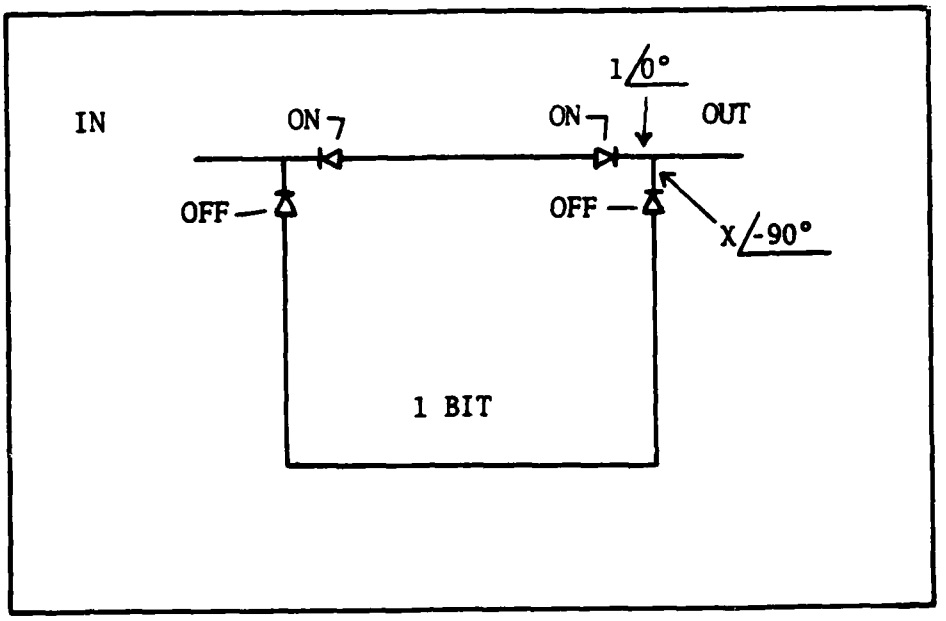

Figure II-9, Time Delay Error From Poor Isolation

vector $1\angle 0^\circ$ and the worst case error is the vector $x\angle -90^\circ$. Addition of these two vectors must produce a vector less than or equal to the maximum allowable error. Stated in mathmatical symbols,

$$1.0\angle 0.0^\circ + x\angle -90^\circ < \text{mag.}\angle 10.8^\circ \qquad (11)$$

Solving equation (11) for x produces a value of 0.1908. Assuming each of the four long paths contributes 1/4 of the total error permissible, the required isolation is then 10 log (.1908/4) = -13.2 db for each path. Since the 4P202 PIN diodes selected each provide 21.3 db of isolation, they are more than adequate.

Power Handling Limits (Ref 7:71-78)

The power handling capability of a microstrip, like that of any other dielectric filled transmission line, is limited by heating caused because of ohmic and dielectric losses and by dielectric breakdown. Increases in temperature due to conductor and dielectric losses limit the average power of the microstrip line, while the breakdown between the strip conductor and ground plane or breakdown of the diodes limits the peak power.

The average power handling capability of microstrip is determined by the temperature rise of the strip conductor and the supporting substrate. The major parameters in the calculation of average power capability are listed below:

1. Transmission line losses,
2. Thermal conductivity of the substrate,
3. Surface area of the strip conductor, and
4. Ambient temperature.

Gupta has derived the following equation for use in calculating the average power handling capability of a microstrip line.

$$\Delta T/P_i = 0.2303h/K[\alpha_c/w_e + \alpha_d/(2w_{eff}(f))] \ ^{o}C/watt \quad (12)$$

where h and K are the thickness of the substate (2.0 mm) and its thermal conductivity (2.0934 watts/m^{o}C), respectively.

W_e, the equivalent width of the strip to account

for the increase in area normal to heat flow lines, is given by

$$w_e = 120 \quad h/(Z_0'(\epsilon_{re}')^{1/2}) \tag{13}$$

In this case, Z_0' and ϵ_{re}' are calculated with ϵ_r replaced by Kd/Ka (the ratio of thermal conductivity of the dielectric to that of air). Here, Kd/Ka = 2.0934/0.024 = 87.23 (Ref 7:73; 13:1628; 18:511). Using 87.23 for ϵ_r in equation (5) gives a value of ϵ_{re}' = 49.69. The microstrip synthesis equations (1) through (3) have been combined into one analysis equation (Z_0 in terms of w/h and ϵ_r) by Gupta and is presented here for the case w/h < 2 (Ref 7:11).

$$Z_0 = (60/((\epsilon_r + 1)/2)^{1/2})\{\ln(8h/w) + ((w/h)^2/32) - (0.5(\epsilon_r - 1)/(\epsilon_r + 1))(0.452 + 0.242/\epsilon_r)\} \tag{14}$$

Now, for w = 0.340 mm, h = 2.0 mm (from Table II-1) and replacing ϵ_r with Kd/Ka, equation (14) gives Z_0' = 32.79. Substituting these known values into equation (13) produces a value for w_e, the effective width for heat flow, of 3.26 mm.

α_c, the conductor loss, is presented for w/h < 1 below (Ref 6:63-64).

$$\alpha_c = 1.38A(R_s/(hZ_0))(32 - (w_e/h)^2) \; / \; (32 + (w_e/h)^2) \text{ db/m} \tag{15}$$

where for $w/h > 1/(2\pi)$

$$w_e/h = w/h + (1.25t/(\pi h))(1 + \ln(2h/t)) \quad (16)$$

and

$$A = 1 + (h/w_e)\{1 + (1/\pi)(\ln(2h/t))\} \quad (17)$$

R_s, the surface resistivity of the strip conductor is given by

$$R_s = (\pi f \mu_0 \rho)^{1/2} \quad (18)$$

where

f = operating frequency

μ_0 = free space permeability

ρ = electrical resistivity

Lee (Ref 10:658) calculated R_s for a gold microstrip conductor and after adding 3% to allow for substrate surface roughness presented

$$R_s = 9.772 \times 10^{-3}(f(GHz))^{1/2} \quad (19)$$

which at the design frequency of 3 GHz provides $R_s = 1.693 \times 10^{-2}$. Assuming a strip conductor thickness (t) of 10 microns and with the other values given in Table II-1, equation (16) can be solved for $w_e/h = 0.18391$. Equation (17) is then, A = 16.807 and equation (15) provides $\alpha_c = 3.918$ db/m.

The dielectric loss, α_d, is given by

$$\alpha_d = 27.3(\epsilon_r/(\epsilon_r - 1))\{(\epsilon_{re} - 1)/(\epsilon_{re})^{1/2}\}(\tan\delta/\lambda_0) \quad (20)$$

Masse (Ref 13:1628) provides an average value of 0.00039 for $\tan\delta$ from over 200 batches of barium tetratitanate he tested. Using this value and the values from Table II-1 produce α_d = 0.4815 db/m.

The density of heat generated by dielectric loss is proportional to the square of the electric field and is a function of frequency. This effective width, $w_{eff}(f)$, depends on the spread of electric field lines and is given by

$$w_{eff}(f) = w + \{(w_{eff}(0) - w)/(1 + (f/f_p)^2)\} \quad (21)$$

where

$$f_p = Z_0/2\mu_0 h \quad (22)$$

and $w_{eff}(0)$ is equal to w_e of equation (13). With f_p = 9.947 GHz, $w_{eff}(f)$ = 3.02 mm at 3 GHz.

With all parameters now known for equation (12), the rise in temperature for this gold microstrip on barium tetratitanate is $\Delta T/P_i$ = 0.282 ^{o}C/watt.

However, the chip PIN diodes mounted on the microstrip are the key elements in determining the power handling limits of this time delay circuit. The thermal resistance,

θ_{jc}, is the ratio of the steady state temperature rise of the diode junction per watt of steady state power dissipated within it. The maximum thermal resistance of the 4P202 PIN diodes is 60 ^{o}C/watt (Ref 16:107).

With the PIN diode attached to the microstrip with silver paint as shown in Figure II-10, the total thermal resistance can be determined as the sum of the separate thermal resistances incurred by heat flow from the junction to the ground plane (Ref 18:512).

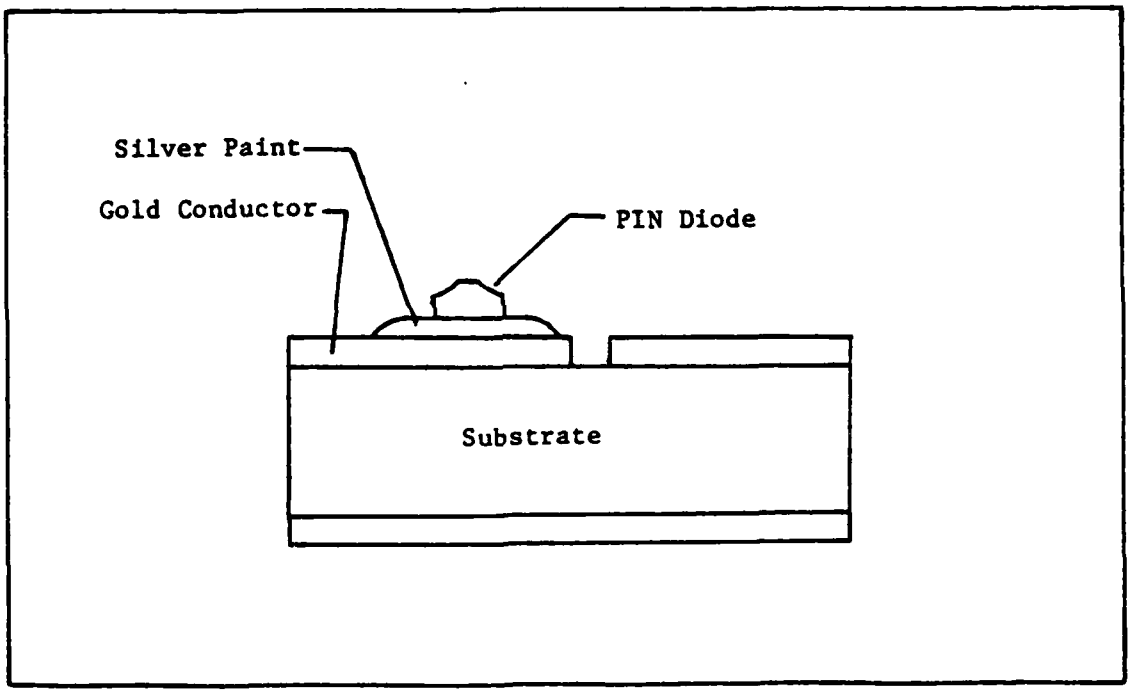

Figure II-10, Cross Section of PIN Diode on Microstrip

Having already determined the RF thermal resistance for the gold microstrip on the substrate, and given the maximum thermal resistance of the PIN diode, all that remains is to

determine the DC thermal resistance of the silver paint, the gold conductor, and the barium tetratitanate substrate. White presents the following equation for thermal resistance calculations (Ref 18:513).

$$\theta_2 = \rho(\text{silver paint})\, 4H_2/(\pi D^2) \qquad (23)$$

With ρ(silver paint), the thermal resistivity, equal to 0.25 ^{o}C cm/watt; H_2, the thickness of the silver paint, approximately 1 mil; and D, the diameter of the junction approximated as the measured diameter of the anode, equal to 6.5 mil, equation (23) produces θ_2 = 2.97 ^{o}C/watt.

The PIN diode and silver paint are mounted on the 0.340 mm wide gold microstrip, which according to equation (13) has an equivalent width for heat flow of 3.26 mm. The shortest length of this section of microstrip (see Figure II-8) is 2.42 mm.

Equation (23) can be rearranged as

$$\Delta T/P_d = \theta = H/(Kw_eL) \qquad (24)$$

where

H = height or thickness

K = thermal conductivity

w_eL = area

With the thermal conductivity of gold equal to 294 watts/m ^{o}C, and the thickness of the gold equal to 10 microns,

equation (24) produces θ_3 = 0.00431 ^{o}C/watt.

In a similar manner, using the same area but with H equal to 2.0 mm and K equal to 2.0934 watts/m ^{o}C, for the barium tetratitanate substrate, equation (24) provides θ_4 = 121.0 ^{o}C/watt.

The total thermal resistance of the circuit is then 60.0 (PIN diode junction) plus 2.97 (silver paint) plus 0.00431 (gold conductor) plus 121.0 (barium tetratitanate), or 183.97 ^{o}C/watt.

The continuous-wave power dissipation is given by the diode manufacturer as

$$P_d = (175 - \text{Operating Temperature})/\theta \qquad (25)$$

In this case, the operating temperature is the ambient temperature plus the temperature rise caused by RF power incident on the microstrip, which from equation (12) is (0.282 ^{o}C/watt)(P_i).

Recalling from a previous section that the insertion loss, IL, at 20 ma is 1.03, the power dissipated in the diode is given by

$$P_d = P_i(1 - 1/IL) \qquad (26)$$

Combining equations (25) and (26) and solving for P_i at 25 ^{o}C, the maximum incident average power limit is 26.6 watts.

In a similar manner, at 125 ^{o}C, the average input power limit is 8.9 watts.

III. Circuit Testing and Fabrication

This chapter describes subcircuit testing of the individual components required on the time delay circuit. Basic transmission lines are examined first, followed by the addition of a series chip capacitor to this transmission line. Next, PIN diodes and inductors are characterized and different spacing to width line ratios are tested for coupling effects. Finally, the diode switching control circuit is presented with fabrication and user descriptions.

Transmission Lines

A good transmission line is fundamental to any time delay circuit, therefore a test transmission line was constructed on a,"3M CuClad 250 GX", substrate. This substrate was three inches by two inches by 60 mils thick and had a relative dielectric constant of 2.5 $\pm$0.05. A one inch wide section of the top copper sheet was removed, using a knife and small pliers, and the dielectric material was sandpapered according to the manufacturer's recommendations. A two inch strip of conductive copper foil for a 50 ohm transmission line was selected from a 3M Microwave Design Aids Kit No. 1000. This 174 mils wide foil line had an adhesive backing and was centered along the three inch side of the sanded substrate, about 1/8 inch from the edge. The substrate and transmission line were then baked for one hour at 100 ^{o}C to improve the adhesion.

Using a Hewlett-Packard 8410A Network Analyzer, an H-P 8743B Reflection-Transmission Test Unit (2.0-12.4 GHz), and an H-P 8414A Polar Display Unit with a Smith Chart screen overlay, the VSWR of this transmission line was read directly from the Smith Chart screen. An H-P 8690B Sweep Ocsillator was configured to sweep from 2.850 to 3.150 GHz and provide the input to the microstrip transmission line. The line was terminated in a 50 ohm load and had a measured VSWR of 1.4. Using a utility knife, the outside corners of the microstrip were then trimmed off at a 45 degree angle, a small portion at a time. The VSWR was monitored during this process and trimming was stopped when the camfered length was approximately equal to the width of the transmission line. The resulting VSWR measured 1.23.

Then a gap, approximately 23 mils wide, was cut in this transmission line. Using a Kulicke and Soffa Model 484 ultrasonic wedge tip wire bonding machine with one mil aluminum wire, the gap was bridged with four bonding wires and the VSWR measured 1.3 as shown in Figure III-1. The bond wires were then removed one at a time, each time taking a VSWR measurement to determine the optimum number of bond wires required to bridge a gap. The output of the network analyzer for this experiment is shown in Figures III-1 through III-5. A summary of the results is shown in Table III-1, and a photograph of the substrate and test jig is shown in Appendix B.

Table III-1, VSWR Measurements of Bond Wire Across Gap in Transmission Line

Number of Bond Wires	VSWR
4	1.3
3	1.25
2	1.5
1	1.8
0	Infinite

Figure III-1, Transmission Line Gap with 4 Bond Wires

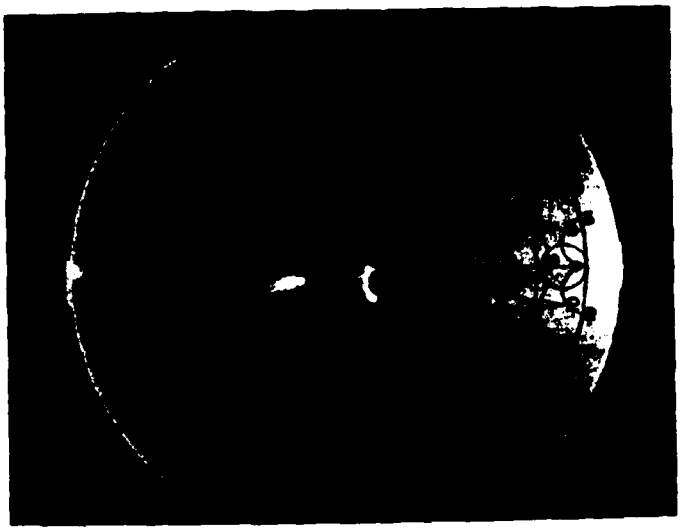

Figure III-2, Transmission Line Gap with 3 Bond Wires

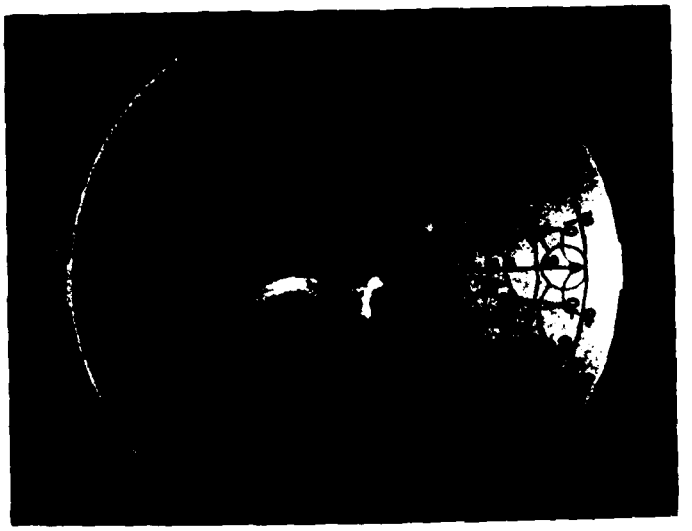

Figure III-3, Transmission Line Gap with 2 Bond Wires

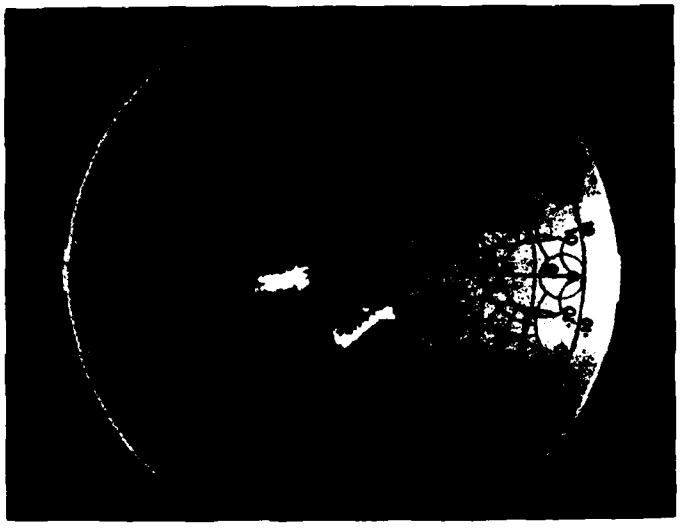

Figure III-4, Transmission Line Gap with 1 Bond Wire

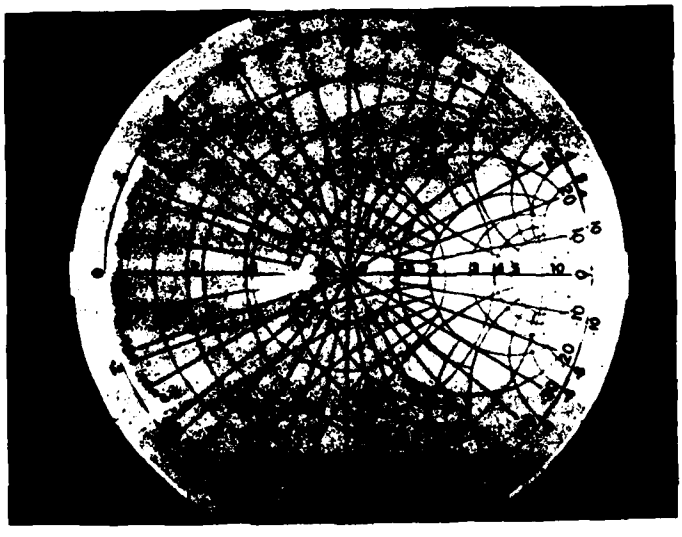

Figure III-5, Transmission Line Gap with 0 Bond Wires

Series Capacitors

To characterize the capacitors required in the time delay circuit design, a 100 pF chip capacitor was attached to one side of the "CuClad" transmission line gap with a small drop of electrical silver paint. The chip capacitor was placed on the drop of silver paint and the paint was allowed to dry before wire bonding from the top side of the capacitor across the gap to the transmission line. As with the transmission line alone, the capacitor was first bonded with four wire bonds, then three, then two, then one, then zero. The VSWR was measured on a network analyzer between each step and the results are shown in Figures III-6 through III-10. A summary of these results is shown in Table III-2.

Table III-2, VSWR Measurements of 100 pF Chip Capacitor in 50 ohm Transmission Line

Number of Bond Wires	VSWR
4	1.25
3	1.3
2	1.4
1	2.2
0	Infinite

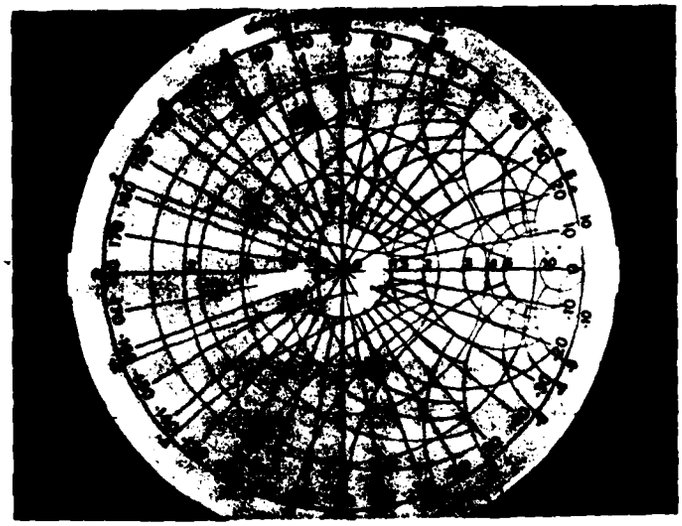

Figure III-6, 100 pF Capacitor with 4 Bond Wires

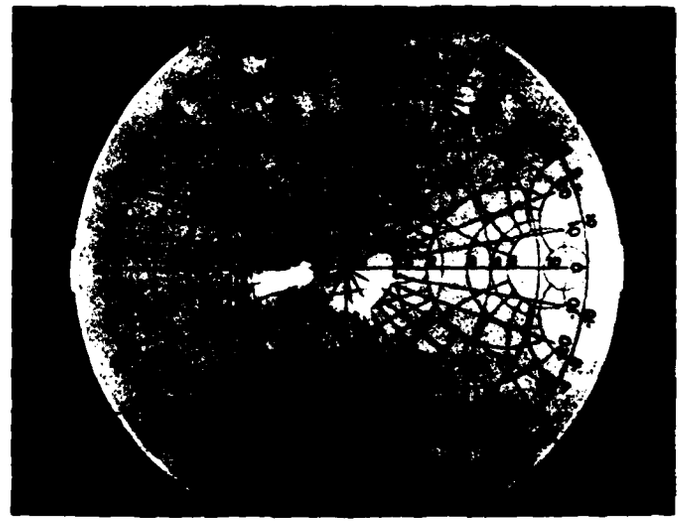

Figure III-7, 100 pF Capacitor with 3 Bond Wires

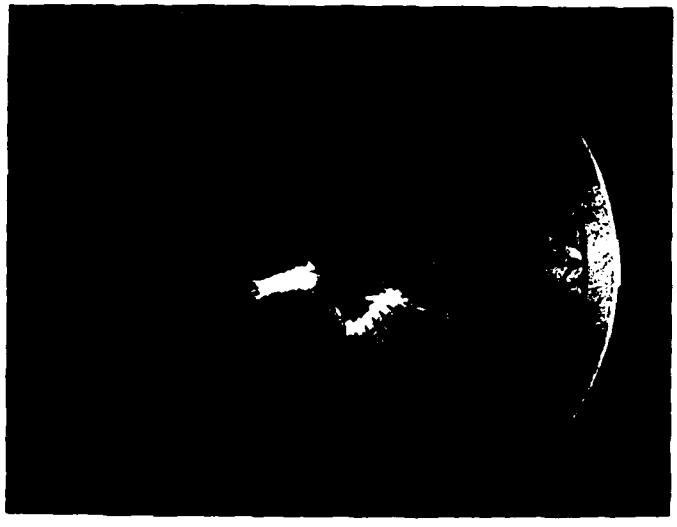

Figure III-8, 100 pF Capacitor with 2 Bond Wires

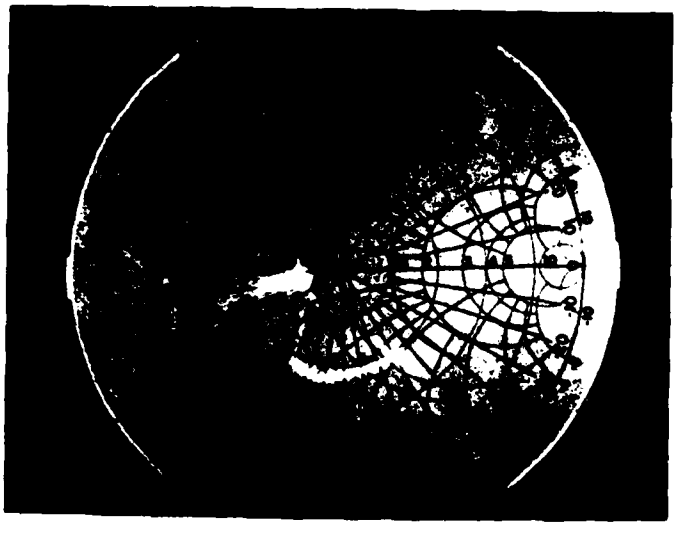

Figure III-9, 100 pF Capacitor with 1 Bond Wire

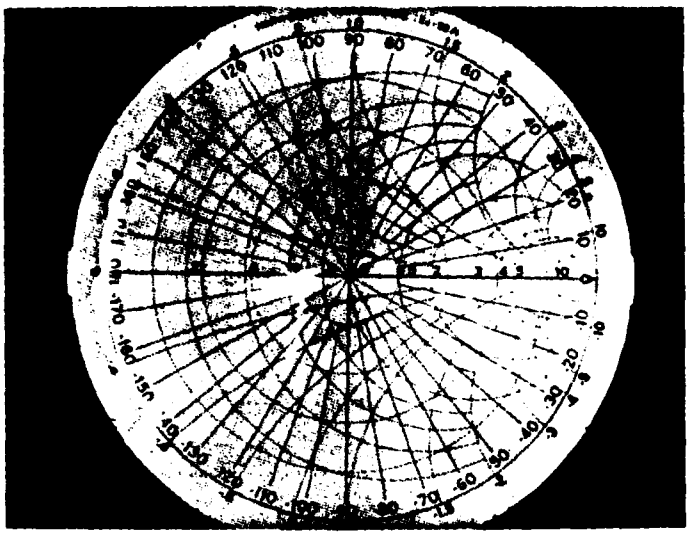

Figure III-10, 100 pF Capacitor with 0 Bond Wires

Series PIN Diodes

Because of a limited stock of 4P202 PIN diodes and an abundance of 4P404 PIN diodes, the latter were used to optimize chip diode mounting techniques. The capacitor and all silver paint was removed from the "CuClad" transmission line and the PIN diode was attached in a similar manner. The cathode was attached with silver paint to one side of the transmission line gap, however, only one wire bond would fit on the anode to bridge across the gap.

SMA bias block adapter Tees were used in the RF test jig, as shown in Figure III-11, to bias the PIN diode.

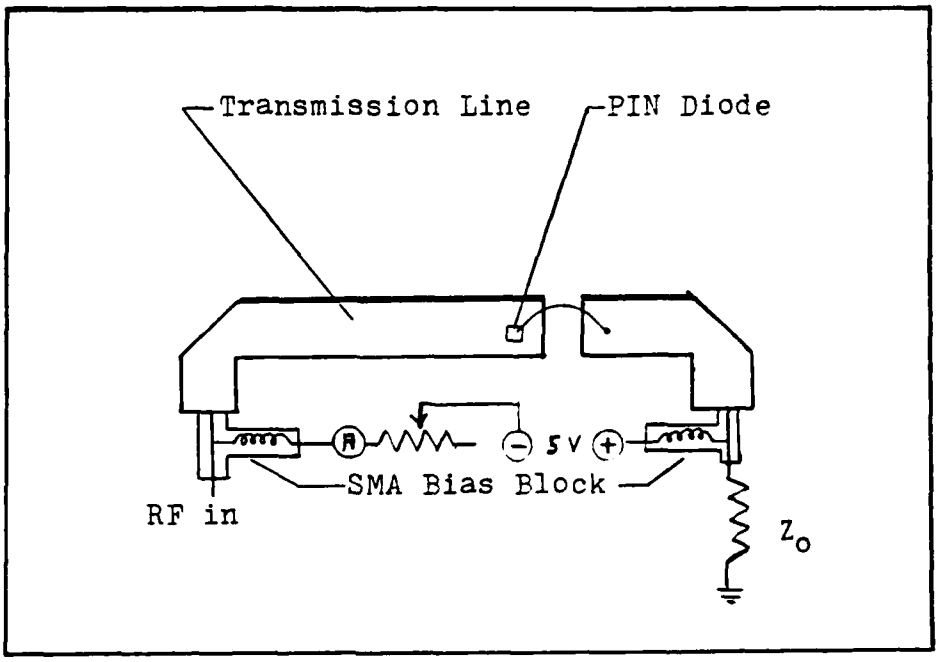

Figure III-11, Forward Bias Configuration for PIN Diode to Pass RF Signal

With the PIN diode forward biased, the measured VSWR was 4.5. Varying the forward bias current from 4 to 100 ma produced no difference in the measured VSWR. Reverse bias produced a good open.

The PIN diode was then removed and physically moved as close to the edge of the gap as possible. A shorter wire bond was made and the measured VSWR improved to 2.4 with 5 volts at 10 ma forward bias current. The network analyzer trace is shown in Figure III-12. With zero volts bias, the measured VSWR was greater than 10, while minus five volts reverse bias was essentially the same. These traces are shown in Figures III-13 and III-14 respectively. A summary

of these results is shown in Table III-3.

Table III-3, VSWR Measurements of PIN Diode

Bias	VSWR (includes bias tee)
5 volts @ 10 ma	2.4
0 volts	>10
-5 volts	>10

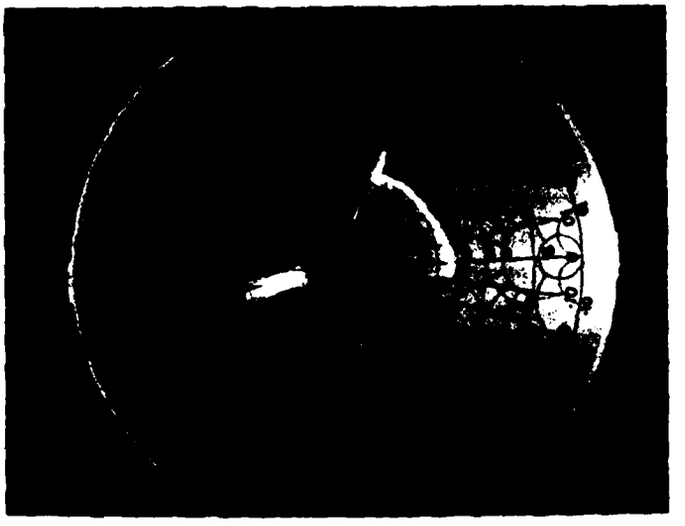

Figure III-12, Forward Biased PIN Diode

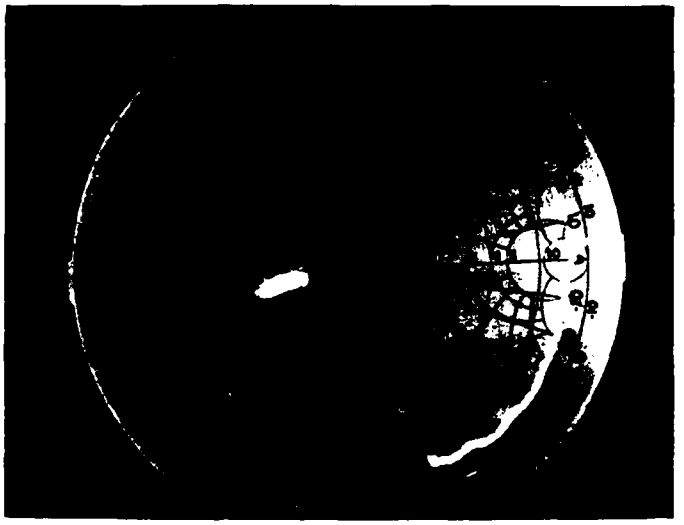

Figure III-13, Zero Volts Bias on PIN Diode

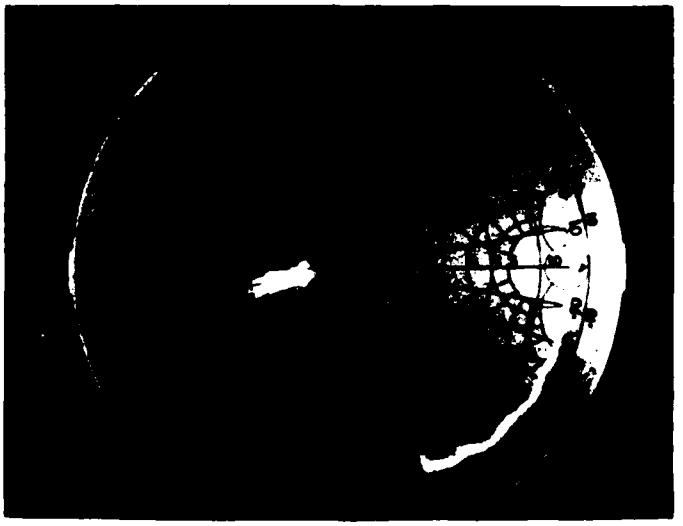

Figure III-14, Minus 5 Volts Bias on PIN Diode

Inductors

The 13 inductors required in the time delay circuit of Figure II-6 must pass the DC bias currents yet provide a good block to the RF signal. An attempt was made to characterize inductors by placing them in shunt to the CuClad transmission line and observing the change in VSWR. However, this method proved unreliable because the changes in VSWR were too small to notice. Therefore, to examine inductors in series, a modified version of Bellacicco's (Ref 1:44) test circuit on alumina was used and is shown in Figure III-15. This 0.025 inch thick alumina substrate had 0.025 inch wide thick film gold transmission lines and a thin film (3.5 micron) copper ground plane. Sets 2 and 3 of section 3 in Figure III-15 were used for inductor characterization.

With 5 turns of 38 gauge wire (4.6 mil diameter) formed around a 0.5 mm pencil lead then attached to transmission line set 2 with silver paint, the network analyzer showed a reactance from -j90 to -j125.

A 3 turn inductor was formed and attached in the same manner to transmission line set 3 and showed an improved reactance of -j105 to -j150. After scraping the excess silver paint from the connection, the reactance improved even further (-j110 to -j175). A photograph of this output was then taken and is shown in Figure III-16.

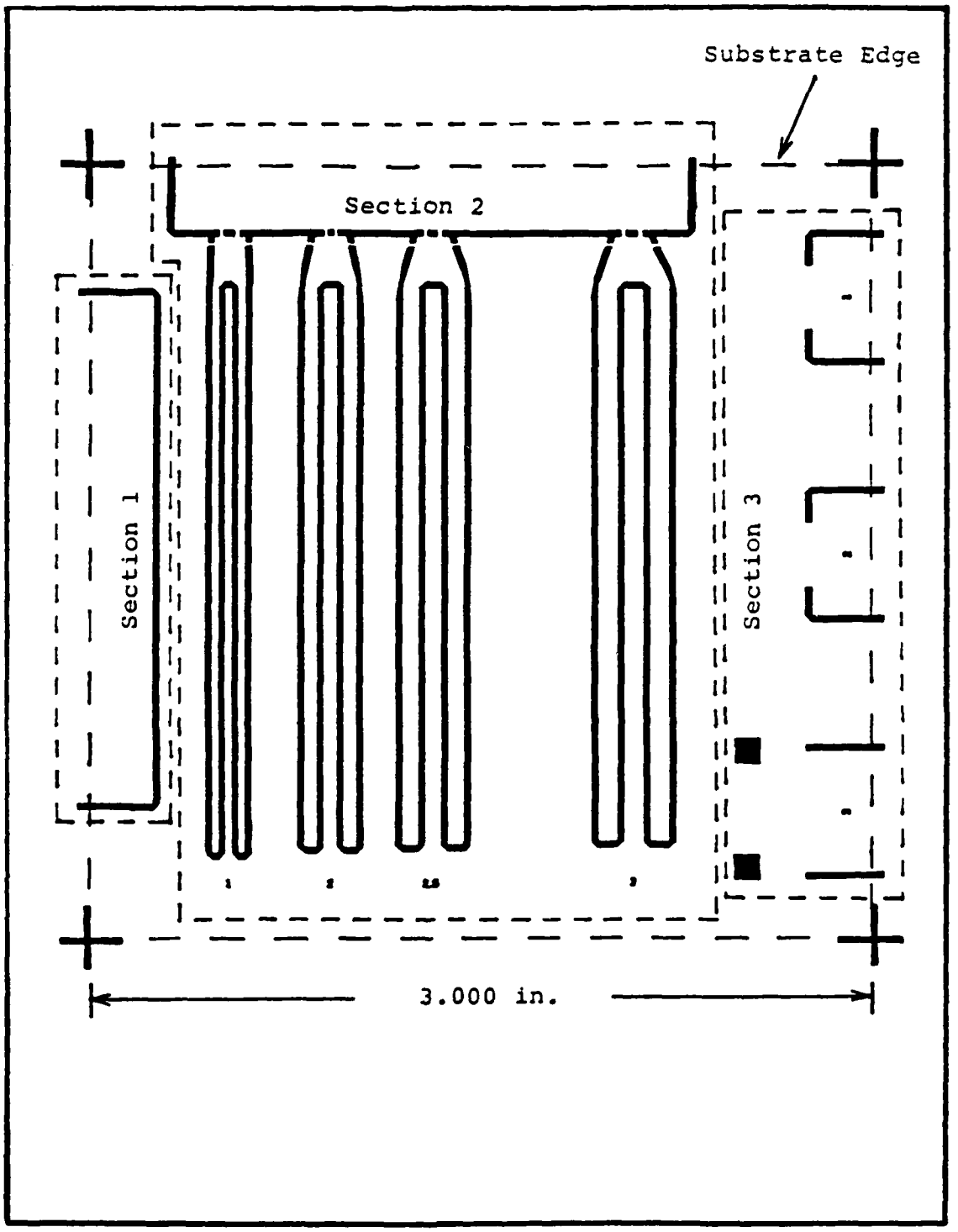

Figure III-15, Gold on Alumina Test Circuit

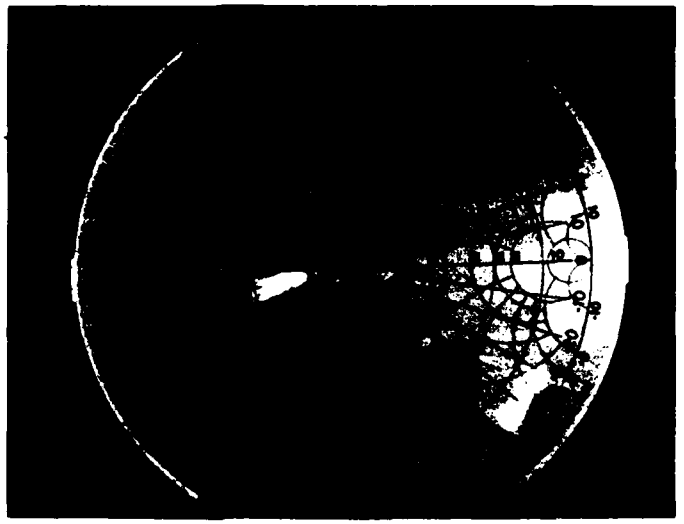

Figure III-16, Reactance of a 3 Turn, 0.5 mm Wound Inductor

Both of these inductors show a reactance that is generally capacitive. At this frequency, this capacitance occurs between the windings, and between the device and ground. In an attempt to reduce this inter-winding capacitance, a one turn inductor, formed and attached as previously described, was tested. This produced a reactance from -j200 to -j500, which, although still capacitive is better than before. This scope trace is shown in Figure III-17.

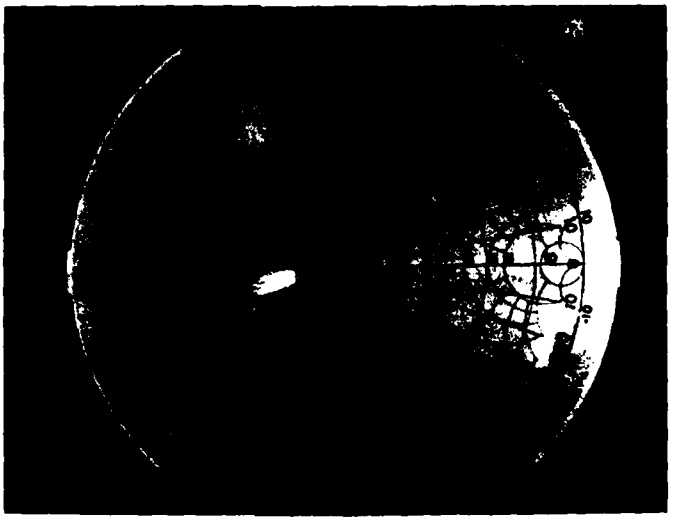

Figure III-17, Reactance of a one turn, 0.5 mm Wound Inductor

For the final test, two zero turn inductors (i.e. straight pieces of wire) were examined. A piece of straight 38 gauge wire was placed flat on the substrate between the two microstrip legs of set 2, attached with silver paint, and tested after scraping away the excess dry paint. On set 3, a single wire bond was made with the ultrasonic bonder using 1 mil aluminum wire.

The piece of straight 38 gauge wire showed a reactance from -j250 to -j1000. This scope trace is shown in Figure III-18. The one mil bond wire produced the best results of all, with a measured reactance from -j500 to +j1000, shown in Figure III-19. Not only is the reactance the best, but

the application method will preclude a lot of potential problems when 13 inductors are applied to the final design on the barium tetratitanate substrate.

A summary of the inductor testing is presented in Table III-4.

Table III-4, Inductor Testing Summary for the Range 2.850 to 3.150 GHz

Type of Inductor	Reactance
5 turn, 0.5 mm Hand Wound	-j90 to -j125
3 turn, 0.5 mm Hand Wound	-j110 to -j175
1 turn, 0.5 mm Hand Wound	-j200 to -j500
Straight 38 Gauge Wire (1/4" long)	-j250 to -j1000
One mil Bond Wire (1/4" long)	-j500 to +j1000

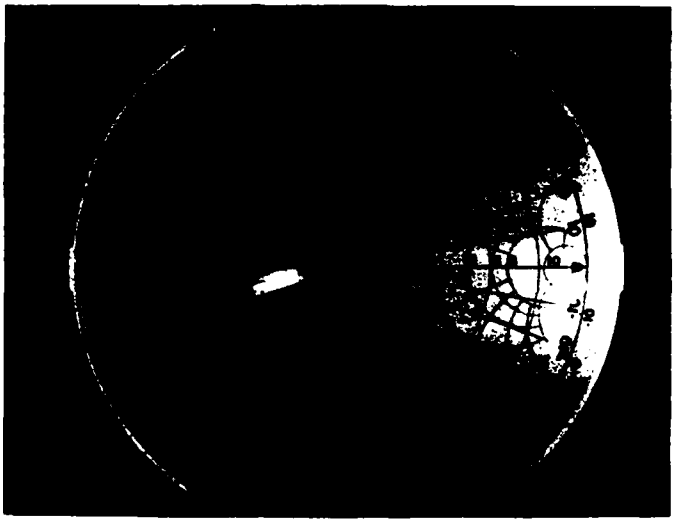

Figure III-18, Reactance of Straight 38 Gauge Wire

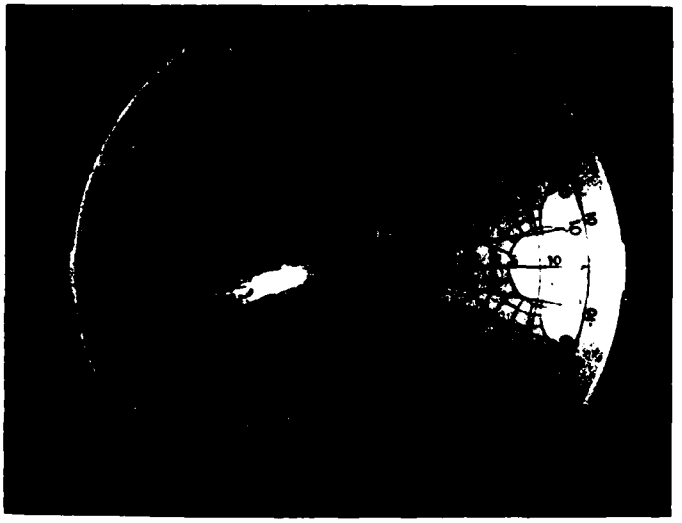

Figure III-19, Reactance of 1 mil Bond Wire

Coupling Effects

Different transmission line spacings as a ratio to the width of the transmission line (s/w ratio) were tested on the alumina test circuit shown in Figure III-15. Minimum coupling between the meandering legs of the transmission line was determined by looking for the minimum VSWR of the different s/w ratios in section 2 of this test circuit.

The length of each long leg in the test circuit is the same and the circuit is designed in such a manner that whichever long leg is chosen, the time delay will be 2.5 nsec. Using two wire bonds per gap, all four s/w ratios were examined with the network analyzer. Additionally, the VSWR of the 1/2 nsec transmission line of section 1 was measured to determine a baseline VSWR. The results of these tests are shown in Figures III-20 through III-24, and summarized in Table III-4.

The poor results obtained from these alumina test circuits could be caused by the 8 wire bonded gaps or by the thickness (t) of the gold conductors. These conductors measure 18 microns thick, on a 0.635 mm high substrate. This t/h ratio of 0.028 is not less than 0.005 as required for the microstrip synthesis equations of Chapter II. However, the general trend that can be determined is the larger the s/w ratio, the better.

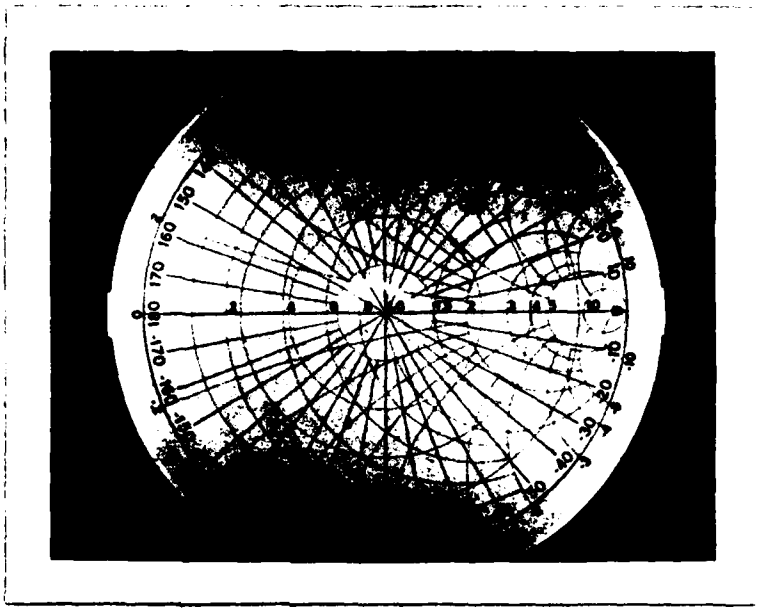

Figure III-20, 1/2 nsec Transmission Line on Alumina

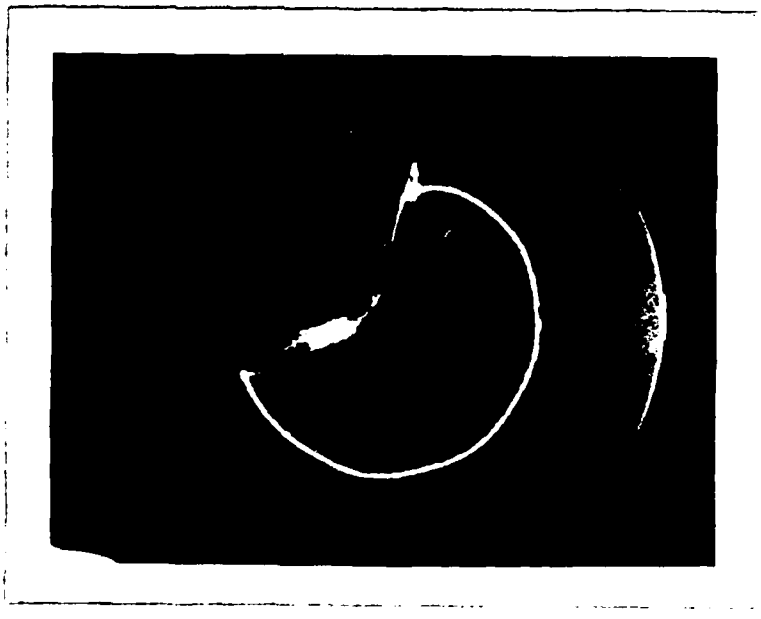

Figure III-21, Alumina Test Circuit, s/w = 3

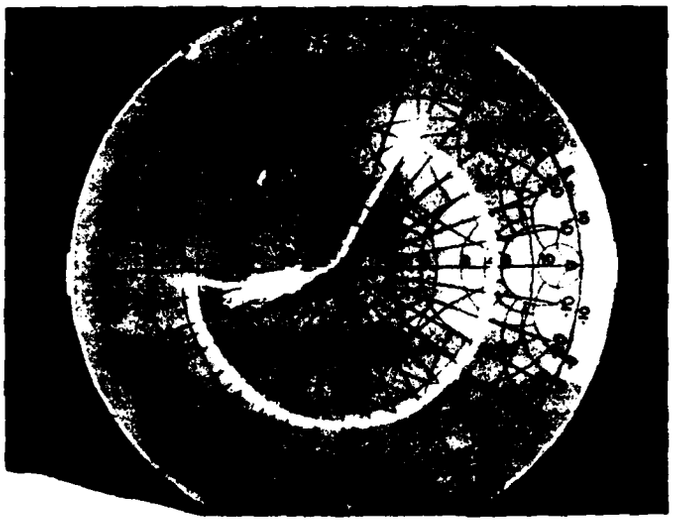

Figure III-22, Alumina Test Circuit, s/w = 2.5

Figure III-23, Alumina Test Circuit, s/w = 2.0

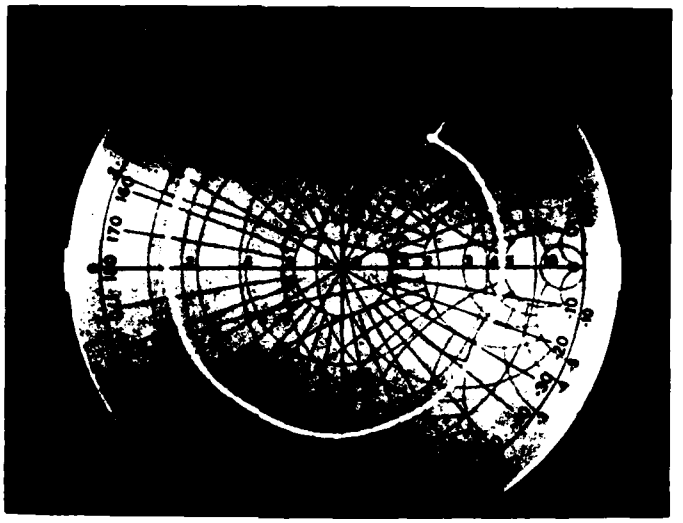

Figure III-24, Alumina Test Circuit, s/w = 1.0

Table III-5, Spacing/Width Ratios on Alumina Test Circuit

s/w	VSWR
~ 1/2 nsec line	1.3
3.0	4.8
2.5	5.0
2.0	8
1.0	6

Diode Switching Control

To select a particular time delay from 1/2 nsec to 8 nsec in 1/2 nsec increments, a diode switching control circuit was constructed and mounted in a separate aluminum chassis box. The control box contains four double-pole double-throw switches (DPDT), a 50 pin wire wrap header, three 3-way binding posts and seven 1/4 watt resistors mounted in a DIP wire wrap socket on a perf board. Only 17 of the bottom 25 pins are used on the wire wrap 50 pin header. The wiring diagram for this control box is shown in Figure III-25. The resistor values are listed in Table II-2, and provide 20 ma forward bias current.

A 50 wire flat ribbon cable carries these control signals to a similar header on the RF test jig, where the 17 pins make pressure contact with the screen printed control lines on the barium tetratitanate substrate (see Figure II-7). A summary of these control lines is presented in Table III-5, and a photograph of the control box, test jig, and substrate is in Appendix C.

One DPDT switch is used for each leg of the time delay circuit. These switches are wired in such a manner that when "A" is high (+5 volts), "$\bar{A}$" is low (-50 volts), and vice-versa. The four switches provide 16 possible time delay settings which are listed in Table III-6. In this project, "0" = -50 volts and "1" = +5 volts.

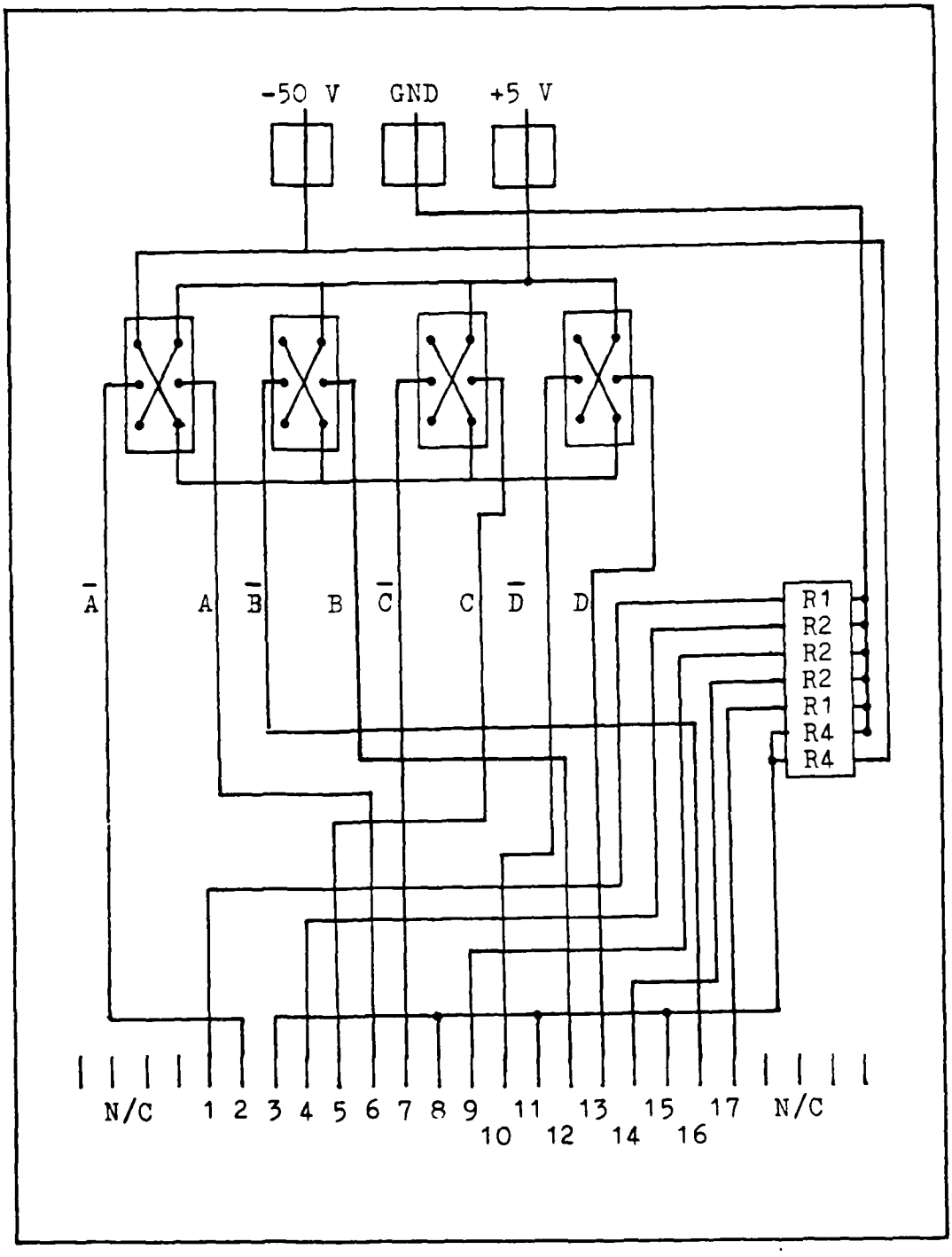

Figure III-25, Wiring Diagram of Diode Control Circuit

Table III-6, Bias Control Line Summary

Pin #	Name	Function
1	R1	220 ohms to Gnd
2	$\overline{A}$	-50 v or +5 v
3	R4	-25 v
4	R2	110 ohms to Gnd
5	C	+5 v or -50 v
6	A	+5 v or -50 v
7	$\overline{C}$	-50 v or +5 v
8	R4	-25 v
9	R2	110 ohms to Gnd
10	$\overline{D}$	-50 v or +5 v
11	R4	-25 v
12	B	+5 v or -50 v
13	D	+5 v or -50 v
14	R2	110 ohms to Gnd
15	R4	-25 v
16	$\overline{B}$	-50 v or +5 v
17	R1	220 ohms to Gnd

Table III-7, Toggle Switch Functions

Switch Position A B C D	Time Delay (nsec)
0 0 0 0	8.0
0 0 0 1	7.5
0 0 1 0	7.0
0 0 1 1	6.5
0 1 0 0	6.0
0 1 0 1	5.5
0 1 1 0	5.0
0 1 1 1	4.5
1 0 0 0	4.0
1 0 0 1	3.5
1 0 1 0	3.0
1 0 1 1	2.5
1 1 0 0	2.0
1 1 0 1	1.5
1 1 1 0	1.0
1 1 1 1	0.5

IV. Barium Tetratitanate Processing

This chapter details the different methods used in an attempt to place microstrip transmission and bias control lines on a barium tetratitanate substrate for the fabrication of a complete time delay circuit.

The initial condition of the substrates and four different processes are presented to explain these attempts. Problems encountered during these processes, including polishing and drilling are explained as they occured.

Initial Substrate Inventory

At the begining of this project, seven 50 mm X 50 mm X 2 mm barium tetratitanate substrates from Thomson CSF were available for experimentation. These grey substrates contained a trace amount of zirconium, added by the manufacturer to obtain a better temperature coefficient. However, the engineering trade off made with this addition is that the substrates now can withstand only 300 ^{o}C maximum. This low maximum temperature rating rules out conventional thick film screen processing to apply a metal conductor on the substrates. For example, to apply a thick film gold conductor requires firing at 980 ^{o}C. Silver and copper thick film conductors require 850 ^{o}C and 650 ^{o}C respectively.

Two of the seven substrates were new and still factory packaged. Five substrates had been used in previous

attempts (last year) to apply a microstrip circuit.

Two of these five used substrates had 0.015 microns (150 Å) of chromium followed by 0.1 microns (1000 Å) of gold evaporated on their surface. An attempt was made last year to then apply a photo resist mask and electroplate the conductor thickness up to four microns of gold. The evaporated gold and chromium between the plated lines would then have been etched away (Ref 1:25; 10:655). However, a low enough plating current could not be maintained and several of the conductors burned through during the electroplating process, i.e. the lines had holes in them, right down to the chromium.

Another two substrates, one with a corner broken off, were received with a layer of oxidized chromium on one side and a vague imprint of the circuit mask.

The fifth used substrate was completely coated with copper that had been applied by electro-less plating. The copper appeared very thin, and a strip had been peeled away by a piece of cellophane tape.

Since additional substrates were not due to arrive until ten months after the begining of this project, these seven substrates were the ones used for experimentation.

Thin Film Ground Plane

After cleaning the two substrates with the gold conductors, 2.5 microns of copper were evaporated on the back side for a ground plane. Then an attempt was made to

electroplate more copper onto this ground plane to obtain approximately 1 mil of copper. During the electroplating process, the electroplated copper adhered well to the evaporated copper, however the evaporated copper began peeling loose from the substrate. This peeling was in sheets (approximately 1/2 square inch) and left the substrate clean.

All gold and copper was then chemically removed by immersion in a commercial solution called, "METEX AUROSTRIP", manufactured by MacDermid, Inc. Both substrates were cleaned by manual scrubbing successively in trichlorethylene, acetone, methanol, and isopropal alcohol. Both substrates were then soaked for 5 minutes in a solution containing 40 ml of hydrogen peroxide and 60 ml of sulfuric acid. Finally, both were rinsed in running de-ionized water (DI water). The chromium remained on one side (the top) of both substrates.

Thin Film Circuit

Using E-beam deposition, both substrates had 2-3 microns of copper evaporated on both sides. The circuit pattern (Figure II-7) was then applied with photo resist on the shiny (buried chromium) side of one substrate and to the dull (no buried chromium) side of the other. As before, during the electroplating process, the evaporated copper began peeling loose from both sides of both substrates. The copper applied to the chromium side blew off while drying

with an air gun. The copper applied to the dull side adhered better, but small flakes were lifting up over the entire surface.

Perhaps copper will never adhere to oxidized chromium. Also, the copper may not adhere to these bare barium tetratitanate substrates because of a poor atomic fit.

Removing Chromium

In an attempt to start over, all five used substrates were placed in a standard chromium etch of 60 ml hydrochloric acid and 20 ml hydrogen peroxide. The copper was removed from the substrates after about three minutes. The four substrates with chromium were left in the etchant for an additional 45 minutes with no noticeable results. All substrates were then rinsed 45 minutes in running DI water.

A second chromium etch was prepared with 50 ml DI water, 25 ml nitric acid, and 5 ml hydrofluoric acid. After agitating the four substrates in this solution for 30 minutes with no noticeable results, the solution was raised to 125 ^{o}C. An additional 15 minutes still had no effect, so the substrates were cooled and rinsed as before.

A third chromium etch, consisting of 60 ml hydrochloric acid and 20 ml nitric acid was then prepared. After soaking the substrates for 15 minutes with no results, 10 ml of hydrofluoric acid was added to the solution. The chromium remained after 10 minutes, so the solution was heated to

125 ^{o}C. An additional 15 minutes still produced no noticeable results so the substrates were allowed to cool and were rinsed as before.

Lee (Ref 10:655) also had difficulty removing chromium from his barium tetratitanate substrates manufactured by Trans. Tech, but was successful with the nitric - hydrofluoric etchant.

Since the chemical etchants did not appear to work, mechanical removal of the chromium seemed to be the only alternative. Using a 12 inch polishing wheel with 1 micron diamond grit on micro-cloth would not even scratch the surface of the chromium. After then attempting 6 micron grit and 45 micron grit unsuccessfully, the chromium was finally removed with a 15 inch wet polishing wheel, using 60 grit (not 60 micron) silicon carbide sandpaper. Even then, approximately 20 minutes grinding time was required. Since the substrate was attached to an aluminum block with double-stick tape, and the block was hand-held against the spinning wheel, the edges and corners of the substrate had more material removed than did the center of the substrate. This crowned substrate would be undesireable for microstrip applications.

A second substrate was attached with double-stick tape to the table of a surface grinder. The machinist set the surface grinder to remove 0.0001 inch increments and the chromium was removed efficiently, leaving a flat substrate.

Since this seemed to be the best way to remove the

chromium, the two remaining substrates were then fastened to the surface grinder table. Then, using 0.0002 inch increments, the machinist began. It was soon obvious that one substrate was thicker than the other. After all chromium had been removed from the thicker one, the grinding wheel was just barely in contact with the other. Since both substrates should be the same height, the machinist continued the automatic 0.0002 inch incremental surface grinding. After a total of 0.005 inches had been removed from the thicker piece, both pieces suddenly and silently cracked into five pieces each. The broken substrates were not warm to the touch, but apparently the stress was too much.

Polishing

To determine the effect on transmission line characteristics, one substrate was polished on one side with an R. H. Strasbaugh "Polish-Master Bench". Automatic, mechanical polishing began with 17 micron diamond grit and proceeded well down through the different grits to 1 micron. During the 1 micron grit polishing, a small chip from the corner of the square substrate broke off and raked across the surface, necessitating a complete starting over. This happened twice, so on the third try, the process was halted after 5 micron grit polishing. Using a profilometer, the surface smoothness was recorded as 1.5 microinches arithmetic average (AA).

A second substrate (one of the new factory sealed ones) was polished in a similar manner on both sides. This surface smoothness then measured 2.2 microinches AA on one side and 2.7 microinches AA on the other.

For comparison, an unpolished substrate (the one that never had chromium applied) measured 20 microinches AA on one side and 18.5 microinches AA on the other. This unpolished substrate, measuring 2.02 mm thick was then used in an electro-less plating procedure.

Electro-less Plating

Electroplating in general requires a conductive material on the substrate to begin the process. Previously this conductive material (copper) was evaporated on in a thin film process. Since this method proved unsuccessful, electro-less plating was attempted for the initial step. In this electro-less plating process, the substrate was dipped in a commercial solution that applied 15×10^{-12} inches of copper to the entire substrate. The substrate was then etched for 15 seconds to remove the oxide and immediately placed in the electroplating tank to plate up enough copper to work with. A film photo resist was then applied by passing the substrate and the film through pressure rollers. The film would not adhere well near the edges, as most plating is done without regard to plating all the way to the edge. After curing, the photo resist film was 1 mil thick, and the substrate was returned to the electroplating tank.

Care must be taken to avoid excess plating and mushrooming over the top of the photo resist. Electroplating tends to plate thicker near the edges of the substrate. Additionally, the substrate must be held in the tank by a conductive clip. This clip "robs" copper that should be plating up on the substrate near the clip. There was also a slight current balance problem, because of the small size of the substrate, in trying to get an even thickness plating on both sides of the substrate. When the plating was thick enough, the photo resist was removed in a tank strip with DuPont, "RISTON Stripper S-1100X", and the substrate was placed in a copper etch until the copper that had been underneath the photo resist was etched away, leaving only the circuit lines.

This entire process was repeated four times on the same substrate. The first three produced a completely unusable circuit and the final try, which was marginal, was the best that could be done.

After the final attempt, the circuit had a small bare hole (approximately 1/4 inch in diameter) in the center of the copper ground plane. This was corrected with a coat of silver paint. On the circuit side, the control line that was closest to the conductive clip was open and the clean substrate was showing through. Since this was a DC control line, it could have been corrected by wire bonding. All four edges were plated, which consequently shorted out the bias control lines and the RF ports. After sanding the

edges with fine sandpaper, the ends of most bias control lines lifted loose from the substrate. Using a DEKTAC profilometer, the plated line thickness (t), measured in a range from 10 microns near the side where the clip was attached, to 20 microns on the side farthest from the clip.

Silver Paint Lines

The substrate that was polished on one side was cleaned for 10 minutes in acetone, then 10 minutes in methanol in an ultrasonic cleaner. Film (Vellum) photo resist was applied as before and an attempt was made to "squeegee" silver paint into the photo resist defined pattern. However, the silver paint attacked the photo resist, leaving a completely unusable mess. The substrate was then stripped and cleaned in preparation for conductive epoxy lines.

Conductive Epoxy Lines

Using thick film techniques, a screen was prepared with the circuit patterm of Figure II-7. Ablebond 36-2, a conductive epoxy from Ablestik Laboratories, was then screen printed onto the substrate and fired at 125 ^{o}C for 1.5 hours. This silver filled conductive epoxy adhered well and looked very good on the polished substrate. However, upon checking with an ohm meter, the lines were all found to be non-conductive. Further investigation revealed the Ablebond 36-2 was manufactured in 1976 and had a shelf life of three months when stored in standard refrigeration or one year if stored at -40 degrees or colder. The jar had been stored in

the freezer compartment of a standard refrigerator and was approximately seven years past its shelf life. The substrate was re-cured at the manufacturer's specification of 130 ^{o}C for one hour to no avail.

A new batch of Ablebond 36-2 was ordered and drilling techniques for barium tetratitanate were explored.

Drilling

The drilling of ceramics has been accomplished for the sponsor of this thesis with a diamond tipped bit and a drill capable of 9000 to 12,000 RPM. A liquid detergent such as "Mr. Clean" was used as the wetting agent/cutting lubricant. The sponsoring laboratory had no experience in drilling barium tetratitanate but such a drilling system was not available here anyway, so laser drilling was attempted.

Using a "Control Laser Model 512", 50 watt, Nd-YAG laser on a broken barium tetratitanate substrate proved unsuccessful. The laser made a pit about 25 mils deep, overheated and shut itself down. After cooling, the exact focus could not be found in the 25 mil diameter pit, so this method was abandoned and an ultrasonic drill was tried.

A Raytheon Model 2-334 Ultrasonic Impact Grinder worked very well on the broken substrate. The correct size bit was fabricated from stainless steel on a machinists lathe, to produce a hole 0.040 inches in diameter. This bit had to be perfectly flat on the tip. In ultrasonic impact drilling, it is the grit in the circulating slurry that does the

actual cutting while the bit is being vibrated with downward pressure.

Using the circuit pattern on the electro-less processed substrate (unpolished) and the non-conductive epoxy processed substrate (polished on one side), four holes were drilled in each substrate (see Figure II-8). The epoxy was then polished off with the "Polish Master Bench", and the copper was etched off as previously described, in preparation for the final circuit.

Final Microstrip Lines

While waiting for the new batch of Ablebond 36-2 to arrive, another silver filled conductive epoxy, "EPO-TEK H20E", manufactured by Epoxy Technology Inc., was found. A small batch of this was prepared to fill all four holes in each substrate and coat the back side for the ground plane. The "EPO-TEK" was then cured according to the manufacturer's specification at 100 ^{o}C for two hours. This epoxy showed good continuity when tested with an ohm meter.

When the Ablebond 36-2 arrived, it was screened on both substrates and cured as previously described. This time the lines were conductive.

To establish a baseline, an attempt was made to wire bond one long leg of the time delay circuit, before adding any discrete components, and measure the VSWR.

The ultrasonic wedge tip bonder would not bond a wire to the conductive epoxy. The epoxy lines felt very "gritty"

and were crowned in the center. After trying several time and power settings on the bonding machine, a fine honing stone was used on the conductive lines to smooth and flatten them. Although this improved the appearance and texture of the lines when viewed under a microscope, wire bonding was still unsuccessful. Re-curing the epoxy was no help so a "Kulicke and Soffa Model 2457, Thermal Compression Pulse Tip Bonder" with 1 mil gold wire was tried. Wire bonding with this gold ball bonder also proved unsuccessful.

A telephone call to Ablestik Laboratories confirmed the fact that you cannot wire bond to an epoxy. All bonding attempts on the "EPO-TEK" ground plane were also unsuccessful.

Since approximately 100 wire bonds must be made to the conductive epoxy transmission and control lines to connect the 43 discrete components, this project appears to be unsuccessfully finished.

V. Conclusions and Recommendations

Conclusions

Microstrip technology can provide an inexpensive, temperature stable variable time delay circuit for use in phased array radar antennas. Microstrip on a barium tetratitanate substrate is one method for producing such a miniature, dependable circuit.

The four-bit loaded switched-line microstrip circuit developed in this thesis can provide a time delay from 1/2 to 8 nsec in 1/2 nsec increments. With PIN diodes used as the switching elements, the circuit will have a maximum phase angle error of less than 10.8 degrees and can handle an input power level of 26.6 watts average at 25 ^{o}C.

Although all attempts to produce this time delay circuit proved futile, because of the difficulty in applying a conductor to barium tetratitanate, they can perhaps serve as a guide for future research on this problem.

Recommendations

On the existing conductive epoxy circuits applied to two separate barium tetratitanate substrates, some type bonding pad should be epoxied to each location that a wire bond is to be made. Although this circuit requires approximately 100 bonding pads (in addition to the 43 discrete components) to be attached with conductive epoxy, after curing and wire bonding, the time delay circuit would

be complete.

Attempts with conductors other than chromium, gold, or copper should be pursued to place a microstrip circuit on a barium tetratitanate substrate.

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Appendix A

Materials and Equipment

The following list of special equipment and materials were used in this thesis project.

1. Network Analyzer (HP 8410A)
   A. Reflection-Transmission Test Unit (HP 8743B)
   B. Polar Display Unit (HP 8414A)
2. Sweep Oscillator (HP 8690B)
   A. 0.1 - 4 GHz Plug-in Unit (HP 8699B)
3. Spectrum Analyzer (AIL 707)
4. Ultrasonic Wedge Tip Bonder (Kulicke and Soffa Model 484)
5. Thermal Compression Pulse Tip Bonder (Kulicke and Soffa Model 2457)
6. Photo-lithographic mask fabrication equipment
7. Thin-film E-Beam vacuum deposition equipment
8. Thick-film circuit fabrication equipment
9. Various polishing wheels
10. Surface grinder
11. Polish-Master Bench (R. H. Strasbaugh Model R6UR-DC-4)
12. Nd-YAG laser drill (Control Laser Model 512)
13. Ultrasonic drill (Raytheon Model 2-334 Impact Grinder)
14. Profilometer (Bendix Type QB Model 18)

15. Surface Profile Measuring System with strip chart (Sloan DEKTAC)
16. Copper clad substrate (3M CuClad 250 GX)
17. Barium tetratitanate substrates
18. Alumina substrates
19. Unpackaged chip PIN diodes, chip capacitors, and chip resistors
20. 38 gauge enameled copper wire

AD-A138 026 A MICROSTRIP TIME DELAY CIRCUIT ON BARIUM TETRATITANATE 2/2
(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH
SCHOOL OF ENGINEERING D A HAHN DEC 83
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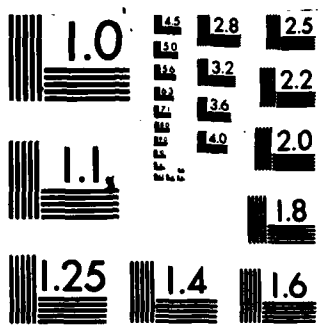

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

Appendix B

Figure B-1, CuClad Test Circuit on RF Test Jig

Appendix C

Figure C-1, Complete Substrate with Diode Control Box

VITA

Danny A. Hahn was born on 3 September 1946 in Fairbury, Illinois. He graduated from high school in Cullom, Illinois in 1964 and enlisted in the U. S. Air Force that same year. After 12 years as an electronics and cryptographic technician, he entered the Airmen's Education and Commissioning Program and received a Bachelor of Science, Electrical Engineering degree from the University of Illinois at Urbana/Champaign in 1976. After receiving a commission through OTS, he served as Chief, Satellite Operations Team, at Sunnyvale AFS, California and as Deputy Commander of the Guam Satellite Tracking Station until entering the School of Engineering, Air Force Institute of Technology in June 1982. He is a member of Eta Kappa Nu and Tau Beta Pi.

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Title: A MICROSTRIP TIME DELAY CIRCUIT ON BARIUM TETRATITANATE

A microstrip time delay circuit, variable from 1/2 to 8 nsec in 1/2 nsec increments at a 3 GHz operation frequency with a 10% bandwidth is presented. The temperature stable, miniature circuit is designed for a 50 X 50 X 2 mm substrate of barium tetratitanate, $BaTi_4O_9$. A PIN diode switching control circuit was fabricated for user selection of the delay time provided by the four-bit loaded switched-line circuit. PIN diodes, chip capacitors, and wound inductors were characterized for this S-Band frequency range. Several different methods and attempts to adhere a conductor to the barium tetratitanate substrate were made and are presented here, however the complete time delay circuit was never fabricated.

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